TELECOM ParisTech

Institut Mines-Télécom

Reliability Assessment Techniques

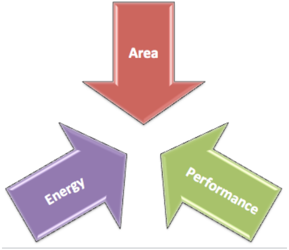
Embedded Systems

Lirida Alves de Barros-Naviner
Master Program

Plan

Outline

Optimized Design of Processors



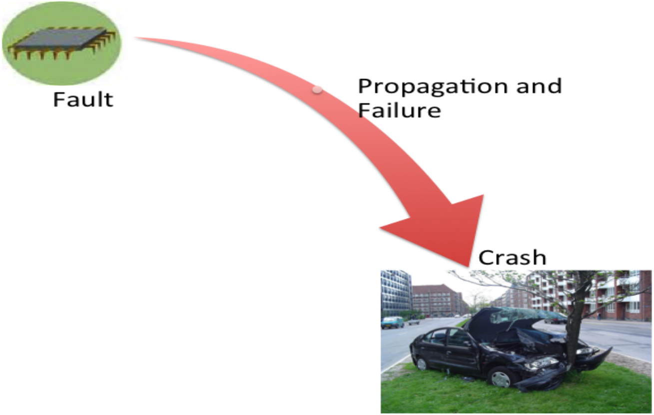
Optimized Design of Processors

How to get **optimized** design of **reliable** processors based on **unreliable** devices?

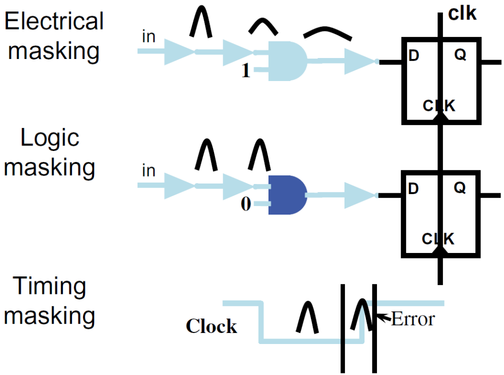
- Risk minimization
- More (than) Moore
- Fabless generalization

Reliability improvement
$\Rightarrow$ penalties !

Fault Propagation



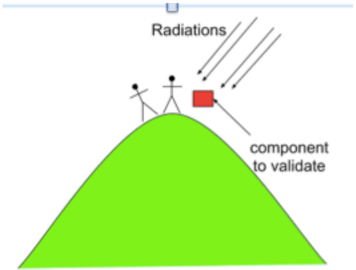
Masking Effects



⇒ Reliability assessment !

Outline

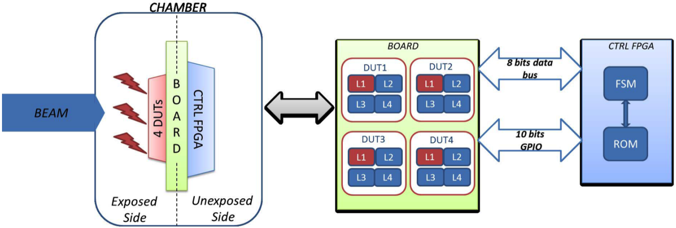
Hardware Fault Injection



Laser Fault Injection

Heavy Ions Test on a μProc

Test vehicle: Leon3 SoC Core

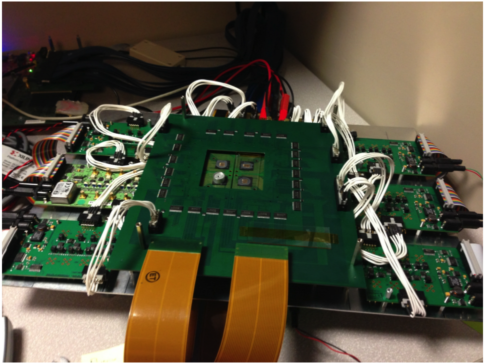


Test Board and Experimental Setup

Heavy Ions Test Result on a 65nm Sparc-V8 Radiation-Hard Microprocessor (IRPS'2014)

Heavy Ions Test on a μProc (cont.)

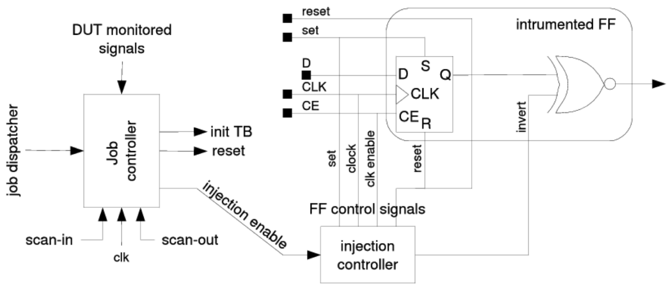
Test vehicle: Leon3 SoC Core



Alpha-particles irradiation for setup validation

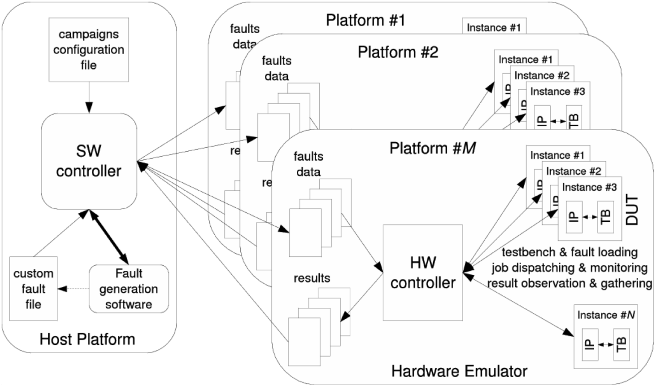
Heavy Ions Test Result on a 65nm Sparc-V8 Radiation-Hard Microprocessor (IRPS'2014)

Fault Injection: HW Emulation



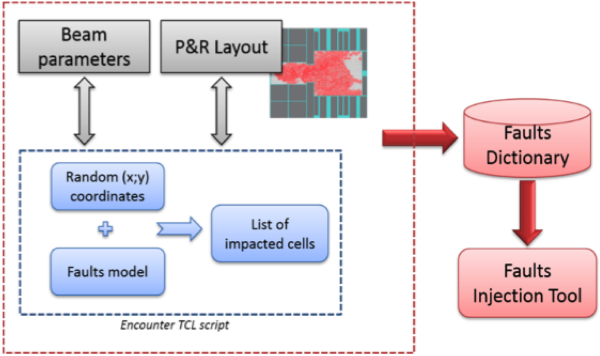
Saboteur. Setup for SEU Fault Injection

Fault Injection: HW Emulation (cont.)



Fault Injection/Emulation Platform.

Fault Injection: Simulation



Platform General Structure

Frequency and Voltage Effects on SER on a 65nm Sparc-V8 Microprocessor Under Radiation Test (IRPS'2015)

Probabilistic Transfer Matrix (PTM)

- A matrix that models the probability of output values according to the occurrence of input values and gate reliability.
- A fault-free gate is modeled by ideal transfer matrix (ITM).

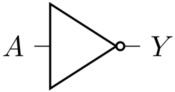
$$\begin{array}{cc} & \text{outputs} \\ \text{inputs} & \begin{bmatrix} \bullet & \bullet & \cdots & \bullet \\ \bullet & \bullet & \cdots & \bullet \\ \vdots & & & \\ \bullet & \bullet & \cdots & \bullet \end{bmatrix} \end{array}$$

probabilities of correct
and incorrect outputs

[1] S. Krishnaswamy, G. Viamontes, I. Markov, and J. Hayes, "Accurate reliability evaluation and enhancement via probabilistic transfer matrices," DATE'05

Examples

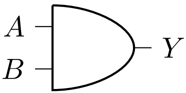
Logic gate NOT



$$PTM_{INV} = \begin{bmatrix} p_0 & q_0 \\ q_1 & p_1 \end{bmatrix} \qquad ITM_{INV} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$$

Examples (cont.)

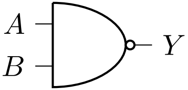
Logic gate AND



$$PTM_{AND} = \begin{bmatrix} q_{00} & p_{00} \\ q_{01} & p_{01} \\ q_{10} & p_{10} \\ p_{11} & q_{11} \end{bmatrix} \qquad ITM_{AND} \begin{bmatrix} 1 & 0 \\ 1 & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix}$$

Examples (cont.)

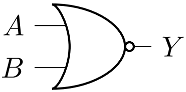
Logic gate NAND



$$PTM_{NAND} = \begin{bmatrix} p_{00} & q_{00} \\ p_{01} & q_{01} \\ p_{10} & q_{10} \\ q_{11} & p_{11} \end{bmatrix} \qquad ITM_{NAND} \begin{bmatrix} 0 & 1 \\ 0 & 1 \\ 0 & 1 \\ 1 & 0 \end{bmatrix}$$

Examples (cont.)

Logic gate NOR



$$PTM_{NOR} = \begin{bmatrix} p_{00} & q_{00} \\ q_{01} & p_{01} \\ q_{10} & p_{10} \\ q_{11} & p_{11} \end{bmatrix} \qquad ITM_{NOR} \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ 1 & 0 \\ 1 & 0 \end{bmatrix}$$

Reliability $\leftrightarrow$ PTM

Definition

$$R = \sum_{(i,j)|ITM(i,j)=1} p(j|i)p(i) = \sum_{(i,j)|ITM(i,j)=1} PTM(i,j)p(i) \qquad (1)$$

Reliability $\leftrightarrow$ PTM

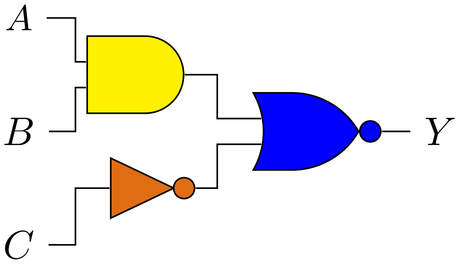
Logic gate NAND

$$R = P\{00,1\} + P\{01,1\} + P\{10,1\} + P\{11,0\}$$

$$P_{AB} = \begin{bmatrix} a_0b_0 \\ a_0b_1 \\ a_1b_0 \\ a_1b_1 \end{bmatrix} \; PTM_{NAND} = \begin{bmatrix} p_{00} & q_{00} \\ p_{01} & q_{01} \\ p_{10} & q_{10} \\ q_{11} & p_{11} \end{bmatrix} \; ITM_{NAND} \begin{bmatrix} 0 & 1 \\ 0 & 1 \\ 0 & 1 \\ 1 & 0 \end{bmatrix}$$

$$R = a_0b_0q_{00} + a_0b_1q_{01} + a_1b_0q_{10} + a_1b_1q_{11}$$

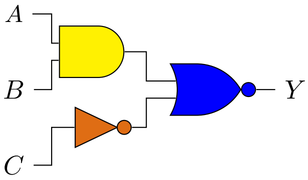
Example



$$p_{ij} = p \text{ and } q_{ij} = q \text{ for all } (i, j)$$

Parallel blocks: Kronecker Product

$$M_1 = \begin{bmatrix} q_{00} & p_{00} \\ q_{01} & p_{01} \\ q_{10} & p_{10} \\ p_{11} & q_{11} \end{bmatrix} \quad M_2 = \begin{bmatrix} p_0 & q_0 \\ q_1 & p_1 \end{bmatrix} \qquad M_{L_1} = M_1 \otimes M_2$$

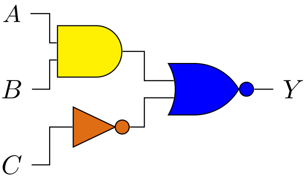


$$\mathrm{M}_{L_1} = \begin{bmatrix} pq & q^2 & p^2 & pq \\ q^2 & pq & pq & p^2 \\ pq & q^2 & p^2 & pq \\ q^2 & pq & pq & p^2 \\ pq & q^2 & p^2 & pq \\ q^2 & pq & pq & p^2 \\ p^2 & pq & pq & q^2 \\ pq & p^2 & q^2 & pq \end{bmatrix}$$

$p_{ij} = p$ and $q_{ij} = q \forall (i, j)$

Series blocks: Scalar Product

$$M_3 = \begin{bmatrix} p_{00} & q_{00} \\ q_{01} & p_{01} \\ q_{10} & p_{10} \\ q_{11} & p_{11} \end{bmatrix} \qquad PTM_{circ} = M_{circ} = M_{L1}.M_3$$



$$\begin{bmatrix} 2p^2q + pq^2 + q^3 & p^3 + p^2q + 2pq^2 \\ p^2q + 3pq^2 & p^3 + 2p^2q + q^3 \\ 2p^2q + pq^2 + q^3 & p^3 + p^2q + 2pq^2 \\ p^2q + 3pq^2 & p^3 + 2p^2q + q^3 \\ 2p^2q + pq^2 + q^3 & p^3 + p^2q + 2pq^2 \\ p^2q + 3pq^2 & p^3 + 2p^2q + q^3 \\ p^3 + 2pq^2 + q^3 & 3p^2q + pq^2 \\ 2p^2q + pq^2 + q^3 & p^3 + p^2q + 2pq^2 \end{bmatrix}$$

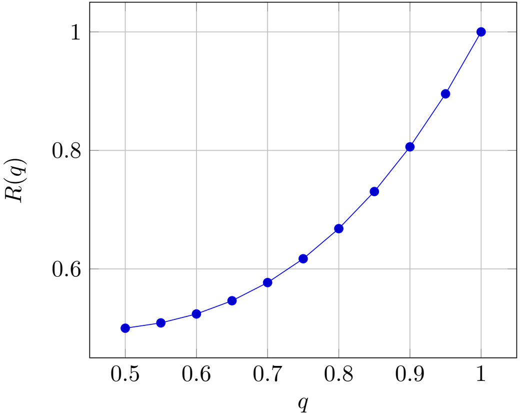
$p_{ij} = p$ and $q_{ij} = q \forall (i, j)$

Reliability Calculation

$$
M_{circ} = \begin{bmatrix}
2p^2q + pq^2 + q^3 & p^3 + p^2q + 2pq^2 \\
p^2q + 3pq^2 & p^3 + 2p^2q + q^3 \\
2p^2q + pq^2 + q^3 & p^3 + p^2q + 2pq^2 \\
p^2q + 3pq^2;; & p^3 + 2p^2q + q^3 \\
2p^2q + pq^2 + q^3 & p^3 + p^2q + 2pq^2 \\
p^2q + 3pq^2 & p^3 + 2p^2q + q^3 \\
p^3 + 2pq^2 + q^3 & 3p^2q + pq^2 \\
2p^2q + pq^2 + q^3 & p^3 + p^2q + 2pq^2
\end{bmatrix}
\qquad
ITM_{circ} = \begin{bmatrix}
1 & 0 \\
0 & 1 \\
1 & 0 \\
0 & 1 \\
1 & 0 \\
0 & 1 \\
1 & 0 \\
1 & 0
\end{bmatrix}
$$

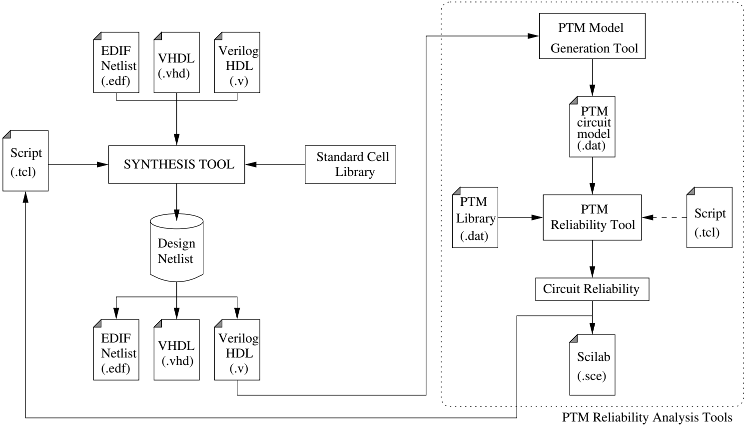
$$
\begin{aligned}
R \quad = \quad & a_0b_0c_0\left(2p^2q + pq^2 + q^3\right) + a_0b_0c_1\left(p^3 + 2p^2q + q^3\right) + \\
& a_0b_1c_0\left(2p^2q + pq^2 + q^3\right) + a_0b_1c_1\left(p^3 + 2p^2q + q^3\right) + \\
& a_1b_0c_0\left(2p^2q + pq^2 + q^3\right) + a_1b_0c_1\left(p^3 + 2p^2q + q^3\right) + \\
& a_1b_1c_0\left(p^3 + 2pq^2 + q^3\right) + a_1b_1c_1\left(2p^2q + pq^2 + q^3\right)
\end{aligned}
$$

System versus Component Reliability



$$P(a_i b_i c_i) = \frac{1}{8} \Rightarrow R_{circ} = q^3 + \frac{3q^2}{4}(-q+1) + \frac{7q}{4}(-q+1)^2 + \frac{1}{2}(-q+1)^3$$

PTM Computing Flow



PTM – Conclusions

- Accurate reliability assessment
- Single and multiple faults
- PTM's size increases exponentially with the number of inputs and outputs
- Intractable computing times and memory storage needs for medium size circuits.
- Scalability problem

Fault State

Definition

Let be the set of n components in a system

$$\mathbb{C} = \{c_0, c_1, c_2, \cdots, c_{n-1}\}$$

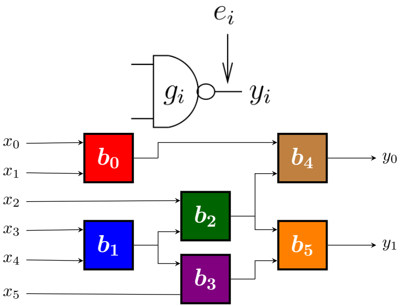
The **fault state of a component** i is defined as

$$f_i = \begin{cases} 0 & \text{if the component } i \text{ is fault-free} \\ 1 & \text{if the component } i \text{ is faulty} \end{cases}$$

for $i = 0, 1, 2, \cdots, n-1$.

Fault Modelling

- $f_i = 1$ inverts expected c_i output
- Remark: a component c_i can be a simple gate g_i or a block of gates $b_i = 1$



System Fault State

Definition

The **system fault state** is defined as

$$\mathbf{f} = f_{n-1} \cdots f_2 f_1 f_0$$

The set of possible $\mathbf{f}$ is

$$\mathbb{F} = \{\mathbf{f}_0, \mathbf{f}_1, \cdots, \mathbf{f}_r, \cdots, \mathbf{f}_{2^{n-1}}\}$$

where $\mathbf{f}_0$ corresponds to all components fault-free.

- $\mathbb{F}_{n:k}$ is a subset of $\mathbb{F}$ of all $\mathbf{f}_r$ with k 1's
- $\mathbb{F}_{n:0} = \{\mathbf{f}_0\}$

System Input and Output

Definition

The system input is defined as

$$\mathbf{x} = x_{m-1} \cdots x_2 x_1 x_0 \text{ where } x_i \in \{0, 1\}$$

The set of possible $\mathbf{x}$ is

$$\mathbb{X} = \{\mathbf{x}_0, \mathbf{x}_1, \cdots, \mathbf{x}_v, \cdots, \mathbf{x}_{2^m-1}\}$$

where $\mathbf{x}_0$ means $x_i = 0$ for all $i = 0, 1, 2, \cdots, m-1$.
The system output is defined as

$$\mathbf{y} = y_{s-1} \cdots y_2 x_1 y_0 \text{ where } y_i \in \{0, 1\}$$

Check Function

Definition

The check system function is defined as

$$h(v,r) = \begin{cases} 1, & \mathbf{y}(\mathbf{x}_v, \mathbf{f}_0) = \mathbf{y}(\mathbf{x}_v, \mathbf{f}_r) \\ 0, & \text{otherwise} \end{cases}$$

or

$$h(v,r) = \overline{\mathbf{y}(\mathbf{x}_v, \mathbf{f}_0) \oplus \mathbf{y}(\mathbf{x}_v, \mathbf{f}_r)}$$

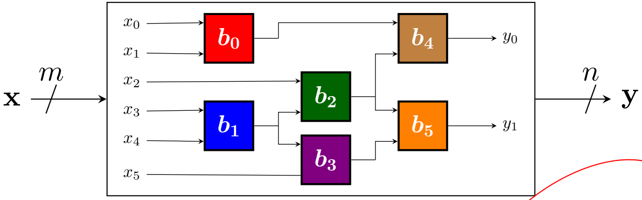
PBR Model

Definition (Probabilistic Binomial Reliability Model)

$$R = \sum_{r=0}^{2^n-1} P\{\mathbf{f}_r\} \sum_{v=0}^{2^m-1} P\{\mathbf{x}_v\} h(v, r)$$

Generalized reliability function for a given circuit with m-bits input and n logic gates (g_i).

Reliability Calculation with PBR

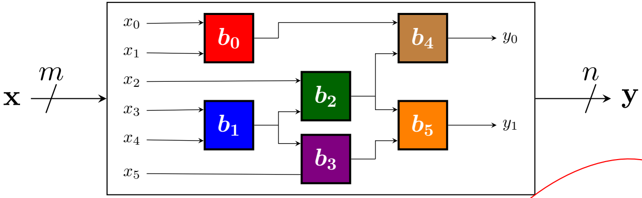


$$R = \sum_{r=0}^{2^n-1} P\{\mathbf{f}_r\} \sum_{v=0}^{2^m-1} P\{\mathbf{x}_v\} \overbrace{(\mathbf{y}(\mathbf{x}_v, \mathbf{f}_0) = \mathbf{y}(\mathbf{x}_v, \mathbf{f}_r))}^{h(v,r)}$$

- Inputs relevance
- Technology & fault relevance
- Logical masking

[1] Reliability Analysis of Combinational Circuits Based on a Probabilistic Binomial Model (NEWCAS'08)

Reliability Calculation with PBR



$$R = \sum_{r=0}^{2^n-1} P\{\mathbf{f}_r\} \sum_{v=0}^{2^m-1} P\{\mathbf{x}_v\} \overbrace{(\mathbf{y}(\mathbf{x}_v, \mathbf{f}_0) = \mathbf{y}(\mathbf{x}_v, \mathbf{f}_r))}^{h(v,r)}$$

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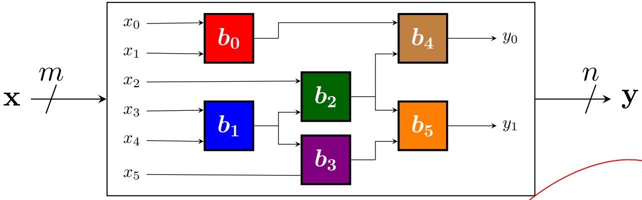

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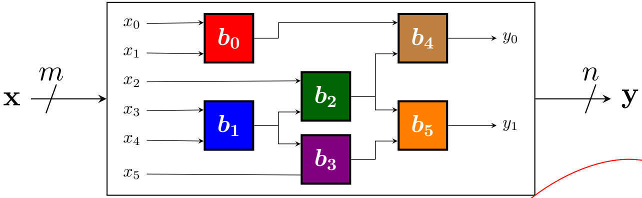


$$R = \sum_{r=0}^{2^n-1} P\{\mathbf{f}_r\} \sum_{v=0}^{2^m-1} P\{\mathbf{x}_v\} \overbrace{\left(\mathbf{y}(\mathbf{x}_v, \mathbf{f}_0) = \mathbf{y}(\mathbf{x}_v, \mathbf{f}_r)\right)}^{h(v,r)}$$

- Inputs relevance
- Technology & fault relevance
- Logical masking

[1] Reliability Analysis of Combinational Circuits Based on a Probabilistic Binomial Model (NEWCAS'08)

PBR Model

k simultaneous faults: R_k

$$
\begin{aligned}
R &= \sum_{r=0}^{2^n-1} P\{\mathbf{f}_r\} \sum_{v=0}^{2^m-1} P\{\mathbf{x}_v\} h(v,r) \\
R_k &= \sum_{l=1}^{C_k^n} P\{\mathbf{f}_{n:k}(l)\} \sum_{j=0}^{2^m-1} P\{\mathbf{x}_j\} \overline{y(\mathbf{x}_j, \mathbf{f}_{n:0}) \oplus y(\mathbf{x}_j, \mathbf{f}_{n:k}(l))}
\end{aligned}
$$

PBR Model

Definition (Independent faults)

$$
\begin{aligned}
R &= \sum_{r=0}^{2^n-1} \prod_{cor_r} q_i \prod_{inc_r} (1-q_i) \sum_{v=0}^{2^m-1} P\{\mathbf{x}_v\} h(v,r) \\
R_k &= \sum_{l=1}^{C_k^n} \prod_{cor_l} q_i \prod_{inc_l} (1-q_i) \sum_{v=0}^{2^m-1} P\{\mathbf{x}_v\} \overline{y(\mathbf{x}_j, \mathbf{f}_{n:0}) \oplus y(\mathbf{x}_j, \mathbf{f}_{n:k}(l))}
\end{aligned}
$$

PBR Model

Definition (Identical probability of faults)

$$
\begin{aligned}
R_k &= \sum_{l=1}^{C_k^n} (1-q)^k q^{n-k} \sum_{v=0}^{2^m-1} P\{\mathbf{x}_v\} \overline{y(\mathbf{x}_j, \mathbf{f}_{n:0}) \oplus y(\mathbf{x}_j, \mathbf{f}_{n:k}(l))} \\
R &= \sum_{k=0}^{n} R_k = \sum_{k=0}^{n} b(q,k) c_k
\end{aligned}
$$

- $b(q,k) = (1-q)^k q^{n-k}$
- c_k are coefficients related to k-faults masking effect

PBR Model (cont.)

k-faults masking coefficient

$$
\begin{aligned}
c_k &= \sum_{l=1}^{C_k^n} \sum_{j=0}^{2^m-1} P\{\mathbf{x}_j\} \overline{y(\mathbf{x}_j, \mathbf{f}_{n:0}) \oplus y(\mathbf{x}_j, \mathbf{f}_{n:k}(l))} \\
&= \sum_{j=0}^{2^m-1} P\{\mathbf{x}_j\} \left(\sum_{l=1}^{C_k^n} \overline{y(\mathbf{x}_j, \mathbf{f}_{n:0}) \oplus y(\mathbf{x}_j, \mathbf{f}_{n:k}(l))} \right)
\end{aligned}
$$

PBR Model

Definition (Uniform probability distribution)

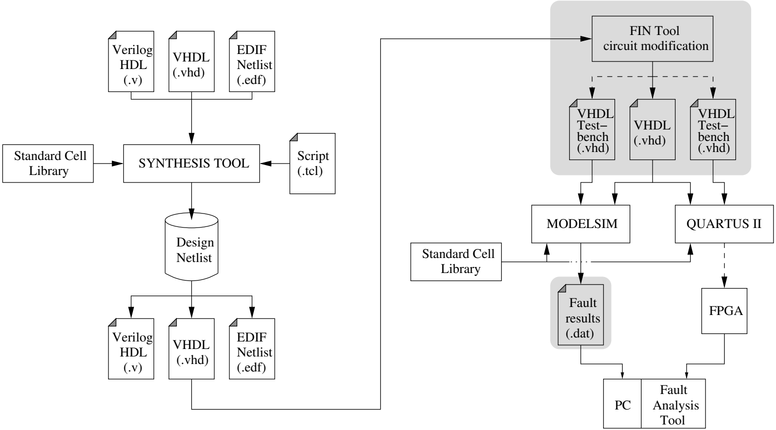
Assuming uniform probability distribution for input vectors $\mathbf{x}$

$$c_k = \frac{1}{2^m} \breve{c}_k$$

$$\breve{c}_k = \sum_{l=1}^{C_k^n} \sum_{j=0}^{2^m-1} \overline{y(\mathbf{x}_j, \mathbf{f}_{n:0}) \oplus y(\mathbf{x}_j, \mathbf{f}_{n:k}(l))}$$

$$R = \frac{1}{2^m} \sum_{k=0}^{n} b(q,k) \left(\breve{c}_k\right)$$

PBR Computing Flow



Simulation or FPGA emulation!

Comparing Performances

PTM and PBR Models

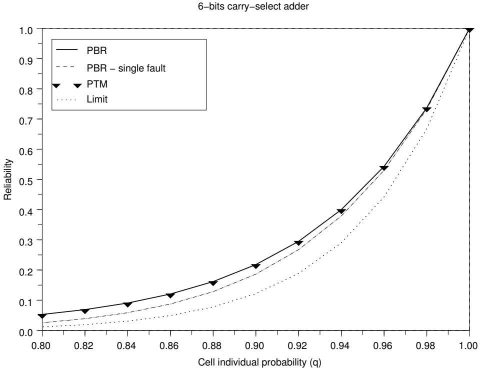
	PTM		PBR		
Adder size	Time (s)	Memory (MB)	Time (s)	Memory (MB)	Mean error (%)
2	0,37	0,133	$< 10^{-3}$	0.027	0.209
3	5,93	1,563	0.04	0.078	0.214
4	104,7	5,819	2.48	0.483	0.301
5	2002.4	255,966	4.91	0.714	0.404
6	-	-	7.94	0.915	0.437
7	-	-	64.12	1.034	0.411
8	-	-	106.69	1.241	0.408

$0.8 < q < 0.99$, 1.7GHz Pentium 4

Accuracy and Scalability Issues

Exhaustive and Relaxed Implementaion

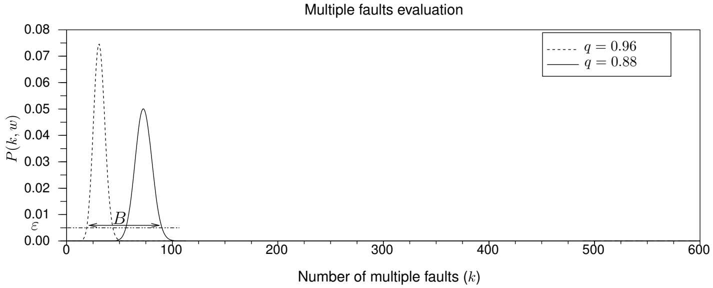
- PBR is as accurate as PTM.



Accuracy and Scalability Issues (cont.)

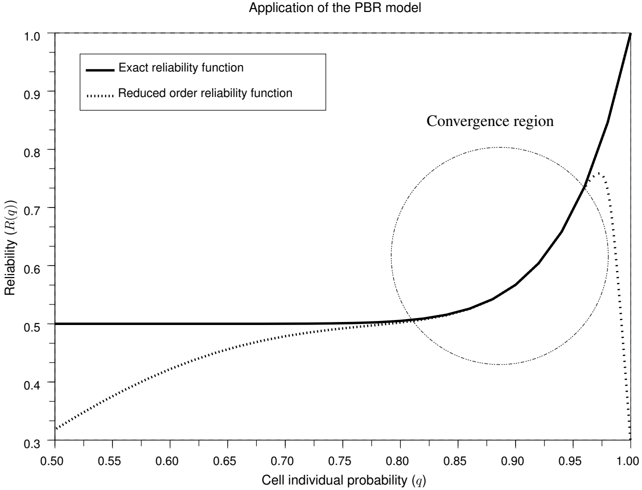
Exhaustive and Relaxed Implementaion

$$P(n,k) = (C_k^n) q^{n-k} (1-q)^k$$



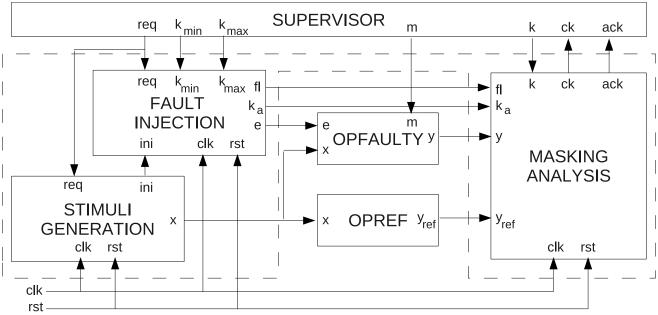
Accuracy and Scalability Issues (cont.)

Exhaustive and Relaxed Implementaion



TELECOM ParisTech

Fault injection/analisys implemented by FPGA



PBR – Conclusions

- Accurate exhaustive approach
  - Gives exact results as PTM model. Requires less memory than PTM.
  - Takes into account all possible inputs and error configurations. Takes into account reconvergent fanouts
- Efficient tradeoffs related to accuracy and exhaustivity can be found
  - Relaxed version of PBR model giving exact (useful) results
- Suitable to be integrated in the design flow
  - Reliability metric becomes a control parameter for the synthesis.
- HW acceleration with FIFA platform is cost and time efficient

Signal Probability Analysis (SPR)

- Fault prone signals s are in one of four different states
- The possible states and respective probabilities are represented in two 2 by 2 matrices

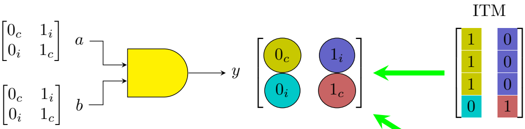
$$s = \begin{bmatrix} 0_c & 1_i \\ 0_i & 1_c \end{bmatrix} \text{ and } P\{s\} = \begin{bmatrix} P\{0_c\} & P\{1_i\} \\ P\{0_i\} & P\{1_c\} \end{bmatrix} \quad (2)$$

$$P\{0_c\} + P\{0_i\} + P\{1_i\} + P\{1_c\} = 1 \quad (3)$$

- The probability matrix $P(s)$ embeds the reliability information

$$R_s = P\{0_c\} + P\{1_c\} \quad (4)$$

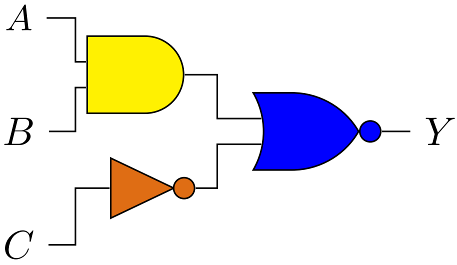
Propagation of Signal Probabilities



$$\begin{bmatrix} 0_c0_c & 0_c1_i & 1_i0_c & 1_i1_i \\ 0_c0_i & 0_c1_c & 1_i0_i & 1_i1_c \\ 0_i0_c & 0_i1_i & 1_c0_c & 1_c1_i \\ 0_i0_i & 0_i1_c & 1_c0_i & 1_c1_c \end{bmatrix} \cdot \begin{bmatrix} q & p \\ q & p \\ q & p \\ p & q \end{bmatrix} = \begin{bmatrix} 0_c0_cq+0_c1_iq+1_i0_cq+1_i1_ip & 0_c0_cp+0_c1_ip+1_i0_cp+1_i1_iq \\ 0_c0_iq+0_c1_cq+1_i0_iq+1_i1_cp & 0_c0_ip+0_c1_cp+1_i0_ip+1_i1_cq \\ 0_i0_cq+0_i1_iq+1_c0_cq+1_c1_ip & 0_i0_cp+0_i1_ip+1_c0_cp+1_c1_iq \\ 0_i0_iq+0_i1_cq+1_c0_iq+1_c1_cp & 0_i0_ip+0_i1_cp+1_c0_ip+1_c1_cq \end{bmatrix}$$

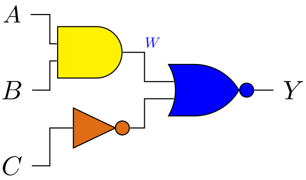
Input signal matrix PTM

Example



$$p_{ij} = p \text{ and } q_{ij} = q \text{ for all } (i, j)$$

L1: Output of Gate NAND



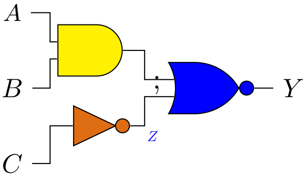
$$AB = \begin{pmatrix} a_{0c}b_{0c} & a_{0c}b_{1i} & a_{1i}b_{0c} & a_{1i}b_{1i} \\ a_{0c}b_{0i} & a_{0c}b_{1c} & a_{1i}b_{0i} & a_{1i}b_{1c} \\ a_{0i}b_{0c} & a_{0i}b_{1i} & a_{1c}b_{0c} & a_{1c}b_{1i} \\ a_{0i}b_{0i} & a_{0i}b_{1c} & a_{1c}b_{0i} & a_{1c}b_{1c} \end{pmatrix}$$

$$PTM = \begin{pmatrix} a_{0c}b_{0c}q + a_{0c}b_{1i}q + a_{1i}b_{0c}q + a_{1i}b_{1i}p & a_{0c}b_{0c}p + a_{0c}b_{1i}p + a_{1i}b_{0c}p + a_{1i}b_{1i}q \\ a_{0c}b_{0i}q + a_{0c}b_{1c}q + a_{1i}b_{0i}q + a_{1i}b_{1c}p & a_{0c}b_{0i}p + a_{0c}b_{1c}p + a_{1i}b_{0i}p + a_{1i}b_{1c}q \\ a_{0i}b_{0c}q + a_{0i}b_{1i}q + a_{1c}b_{0c}q + a_{1c}b_{1i}p & a_{0i}b_{0c}p + a_{0i}b_{1i}p + a_{1c}b_{0c}p + a_{1c}b_{1i}q \\ a_{0i}b_{0i}q + a_{0i}b_{1c}q + a_{1c}b_{0i}q + a_{1c}b_{1c}p & a_{0i}b_{0i}p + a_{0i}b_{1c}p + a_{1c}b_{0i}p + a_{1c}b_{1c}q \end{pmatrix}$$

$$\begin{aligned} w_{0c} &= a_{0c}b_{0c}q + a_{0c}b_{0i}q + a_{0c}b_{1c}q + a_{0c}b_{1i}q + a_{0i}b_{0c}q + a_{0i}b_{1i}q + \\ &\quad a_{1c}b_{0c}q + a_{1c}b_{1i}p + a_{1i}b_{0c}q + a_{1i}b_{0i}q + a_{1i}b_{1c}p + a_{1i}b_{1i}p \\ w_{0i} &= a_{0i}b_{0i}q + a_{0i}b_{1c}q + a_{1c}b_{0i}q + a_{1c}b_{1c}p \\ w_{1c} &= a_{0i}b_{0i}p + a_{0i}b_{1c}p + a_{1c}b_{0i}p + a_{1c}b_{1c}q \\ w_{1i} &= a_{0c}b_{0c}p + a_{0c}b_{0i}p + a_{0c}b_{1c}p + a_{0c}b_{1i}p + a_{0i}b_{0c}p + a_{0i}b_{1i}p + \\ &\quad a_{1c}b_{0c}p + a_{1c}b_{1i}q + a_{1i}b_{0c}p + a_{1i}b_{0i}p + a_{1i}b_{1c}q + a_{1i}b_{1i}q \end{aligned}$$

$$\boxed{W = \begin{pmatrix} w_{0c} & w_{1i} \\ w_{0i} & w_{1c} \end{pmatrix}}$$

L1: Output of Gate NOT



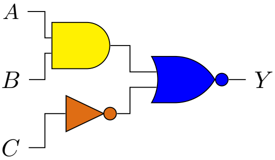
$$C = \begin{pmatrix} c_{0c} & c_{1i} \\ c_{0i} & c_{1c} \end{pmatrix}$$

$$PTM = \begin{pmatrix} c_{0c}p + c_{1i}q & c_{0c}q + c_{1i}p \\ c_{0i}p + c_{1c}q & c_{0i}q + c_{1c}p \end{pmatrix}$$

$$\begin{aligned} z_{0c} &= c_{0i}p + c_{1c}q \\ z_{0i} &= c_{0c}p + c_{1i}q \\ z_{1c} &= c_{0c}q + c_{1i}p \\ z_{1i} &= c_{0i}q + c_{1c}p \end{aligned}$$

$$\boxed{Z = \begin{pmatrix} c_{0i}p + c_{1c}q & c_{0i}q + c_{1c}p \\ c_{0c}p + c_{1i}q & c_{0c}q + c_{1i}p \end{pmatrix}}$$

L2: Output of Gate NOR



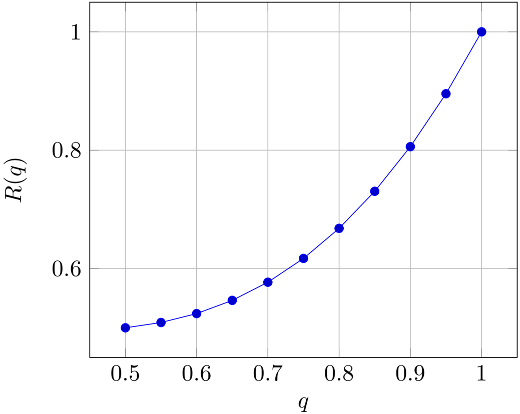
$$WZ = \begin{pmatrix} 3q^2/8 & 3q(-q+1)/8 & 3q(-q+1)/8 & 3(-q+1)^2/8 \\ 3q(-q+1)/8 & 3q^2/8 & 3(-q+1)^2/8 & 3q(-q+1)/8 \\ q(-q+1)/8 & (-q+1)^2/8 & q^2/8 & q(-q+1)/8 \\ (-q+1)^2/8 & q(-q+1)/8 & q(-q+1)/8 & q^2/8 \end{pmatrix}$$

$$PTM = \begin{pmatrix} \frac{3p}{8}q^2 + \frac{3q^2}{4}(-q+1) + \frac{3q}{8}(-q+1)^2 & \frac{3p}{4}q(-q+1) + \frac{3p}{8}(-q+1)^2 + \frac{3q^3}{8} \\ \frac{3p}{8}q(-q+1) + \frac{3q^3}{8} + \frac{3q^2}{8}(-q+1) + \frac{3q}{8}(-q+1)^2 & \frac{3p}{8}q^2 + \frac{3p}{8}q(-q+1) + \frac{3p}{8}(-q+1)^2 + \frac{3q^2}{8}(-q+1) \\ \frac{pq}{8}(-q+1) + \frac{q^3}{8} + \frac{q^2}{8}(-q+1) + \frac{q}{8}(-q+1)^2 & \frac{pq^2}{8} + \frac{pq}{8}(-q+1) + \frac{p}{8}(-q+1)^2 + \frac{q^2}{8}(-q+1) \\ \frac{p}{8}(-q+1)^2 + \frac{q^3}{8} + \frac{q^2}{4}(-q+1) & \frac{pq^2}{8} + \frac{pq}{4}(-q+1) + \frac{q}{8}(-q+1)^2 \end{pmatrix}$$

$$\begin{aligned} y_{0c} &= \frac{5q^3}{8} + \frac{3q^2}{4}(-q+1) + q(-q+1)^2 + \frac{1}{8}(-q+1)^3 \\ y_{0i} &= \frac{9q^2}{8}(-q+1) + \frac{3q}{8}(-q+1)^2 \\ y_{1c} &= \frac{3q^3}{8} + \frac{3q}{4}(-q+1)^2 + \frac{3}{8}(-q+1)^3 \\ y_{1i} &= \frac{9q^2}{8}(-q+1) + \frac{7q}{8}(-q+1)^2 + \frac{1}{2}(-q+1)^3 \end{aligned}$$

$$\boxed{Y = \begin{pmatrix} y_{0c} & y_{1i} \\ y_{0i} & y_{1c} \end{pmatrix}}$$

System versus Component Reliability



$$P(a_i b_i c_i) = \frac{1}{8} \Rightarrow R_{circ} = q^3 + \frac{3q^2}{4}(-q+1) + \frac{7q}{4}(-q+1)^2 + \frac{1}{2}(-q+1)^3$$

SPR Model

Dealing with the effect of reconvergence

- Dynamic Weighted Averaging Algorithm – DWAA (Linear complexity)
- Multi-pass Algorithm – MP (Linear to exponential complexity)
- Conditional Probability Method – CPM (Linear complexity)

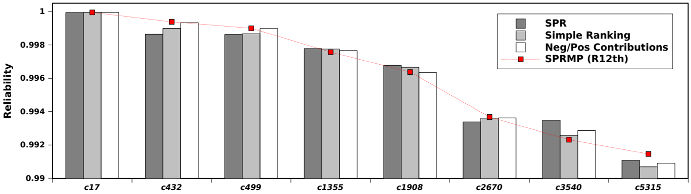
Accuracy & Complexity: Some Results

	PBR		PTM		SPR		SPR_MP	
	$t(s)$	$\epsilon(\%)$	$t(s)$	$\epsilon(\%)$	$t(s)$	$\epsilon(\%)$	$t(s)$	$\epsilon(\%)$
C17	3.3	0.0	0.008	0.0	0.004	4.51	0.02	0.0
CRA 4b	3.83	0.0	287.65	0.0	0.004	13.93	22.98	0.0
CRA 8b	50684	0.0	-	-	0.004	10.19	29218	0.0

First Order Fanout Analysis (SPR+)

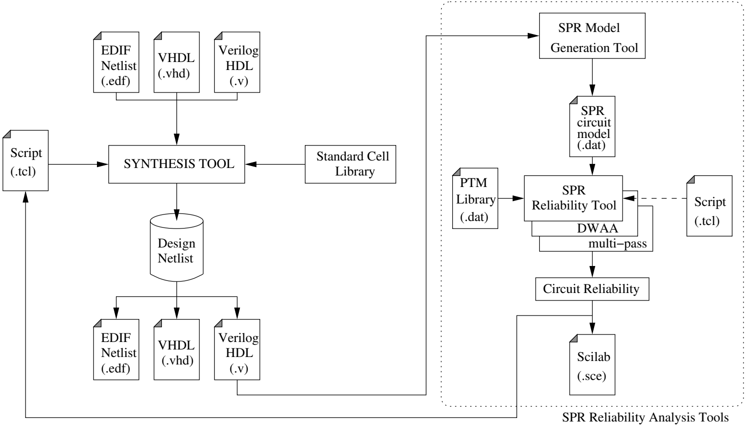
Profile of the Fanout Nodes

$$D(f) = |R_1(f) - R_0| \text{ and } f \text{ has } \begin{cases} \text{High impact,} & \text{if } D(f)/D_{max} > 0.8 \\ \text{Medium impact,} & \text{if } D(f)/D_{max} > 0.2 \\ \text{Low impact,} & \text{otherwise} \end{cases}$$



[1] Reliability Assessment of Combinational Logic Using First-Order-Only Fanout Reconvergence Analysis (MWSCAS'13)

SPR Computing Flow

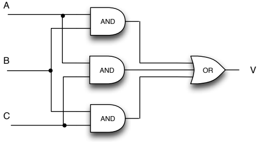


[1] A Tool for Signal Reliability Analysis of Logic Circuits (DATE'09)

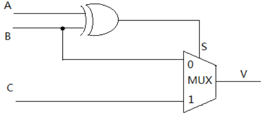
Outline

SPR – Effect of Voter's Reliability

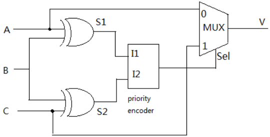
Classical

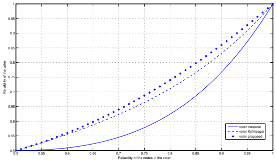


NewCAS(2010)



Kshirasgar(2009)





MTBF Prediction

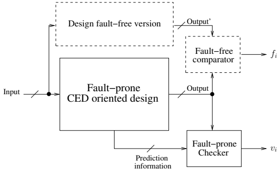
Functional Simulation + Fault Injection Scheme

Example (PBR Implementation)

4-bit Adder	Individual cell $MTBF_i$(hours)			
	10^{12}	10^{9}	10^{6}	10^{3}
RCA	$1.09 \cdot 10^{11}$	$1.10 \cdot 10^{8}$	$1.08 \cdot 10^{5}$	109
CSA	$1.03 \cdot 10^{11}$	$1.07 \cdot 10^{8}$	$1.06 \cdot 10^{5}$	106
CLA	$0.68 \cdot 10^{11}$	$0.66 \cdot 10^{8}$	$0.71 \cdot 10^{5}$	70
SD	$0.20 \cdot 10^{11}$	$0.18 \cdot 10^{8}$	$0.26 \cdot 10^{5}$	21

Analysis of CED Schemes

PBR: Functional Simulation + Fault Injection Scheme



ξ : The checker indicates a valid operation when the outputs are correct.

τ : The checker indicates a non-valid operation when the outputs are correct.

ψ : The checker indicates a valid operation when the outputs are incorrect.

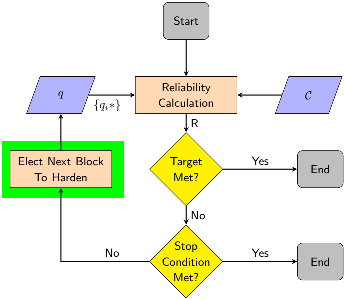
χ : The checker indicates a non-valid operation when the outputs are incorrect.

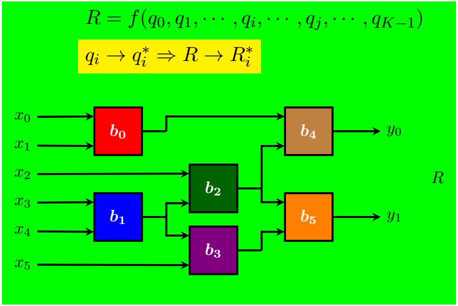
$$\begin{cases} p(f_i = 1, v_i = 1) = p(\xi) \\ p(f_i = 1, v_i = 0) = p(\tau) \\ p(f_i = 0, v_i = 1) = p(\psi) \\ p(f_i = 0, v_i = 0) = p(\chi) \end{cases}$$

Effective reliability: $\Re = p\,(\xi | \xi \cup \psi)$

Time penalty: $\Gamma = p\,(\tau \cup \chi)$

Selective Hardening

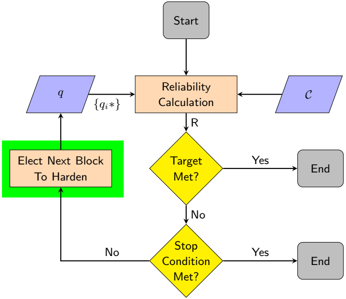


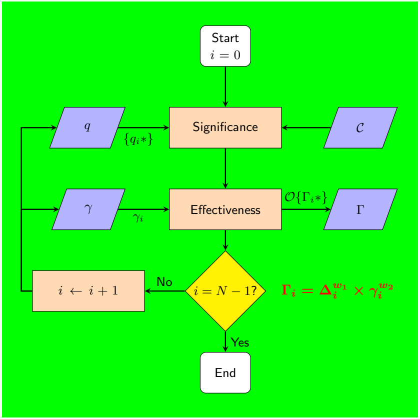


- Sensitivity to reliability change: $\sigma_i = \partial R / \partial q_i$
- Impact of reliability improvement $q_i \rightarrow q_i^*$: $\Delta_i = R_i^* - R$
- Easiness to harden: $\gamma = f(A, P, T)$

[1] Reliability analysis based on significance (CMTA'11)

Selective Hardening





- New partial ordering is needed after hardening a block

[1] Reliability analysis based on significance (CMTA'11)

Outline

Conclusions

- Reliability issues and challenges

- Need of cost-effective fault tolerant architectures
- Need of efficient assessment approaches

- Main issues of reliability assessment approaches
  - Scalability: accuracy, complexity
  - Design flow integration