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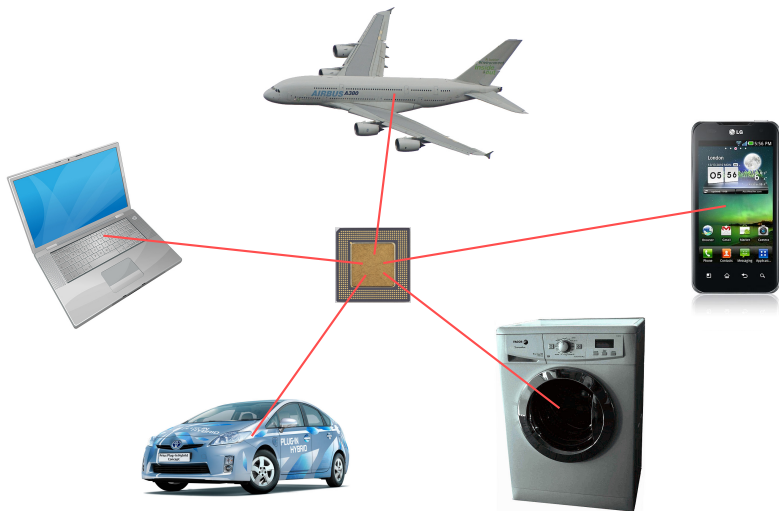
Formal Hardware Verification

Conception des systèmes sur puces

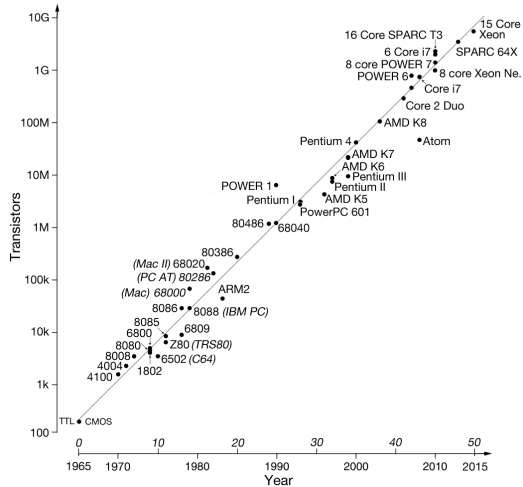
Ulrich Kühne
2016/2017



Motivation

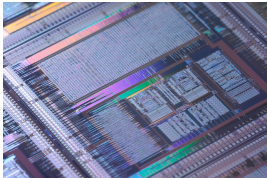


Motivation



[Source: www.elektormagazine.com/articles/moores-law]

Motivation



[© photo by mark.size]

- Transistor count of **> 3 billion**
- Gate level models are **huge**
- Big designer teams (several hundreds)
- Big **correctness** issues
- Late bugs are extremely expensive

The First Bug (1947)

9/9

0800 Andam started

1000 stopped - andam ✓

1300 (032) MP-MC ~~2.130476415~~ 2.130476415 (2) 4.615925059 (-2)

(033) PRO 2 2.130476415

convd 2.130476415

Relays 6-2 in 033 failed speed test

in relay "no test"

Relays changed

1100 Started Cosine Tape (Sine check)

1525 Started Multi-Adder Test.

1545

Relay #70 Panel F (moth) in relay.

First actual case of bug being found.

1630 Andam started.

1700 closed down.

Relay 2145
Relay 2370

[Photo: U.S. Naval Historical Center]

Motivation

The Pentium FDIV Bug (1994)

let $x = 4195835$, $y = 3145727 \Rightarrow x - \frac{x}{y} \cdot y = 256$

- Bug in floating point unit $\Rightarrow$ \$ 450 Mio. loss for Intel

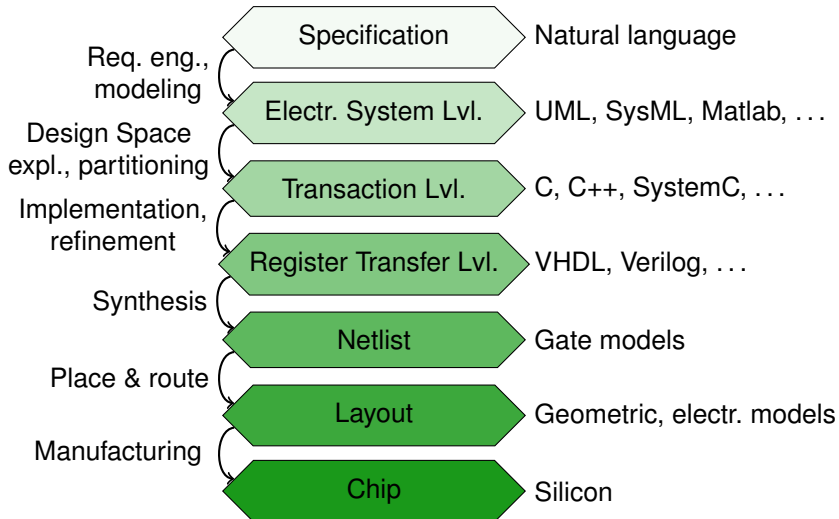
820 Chipset MTH Bug (2000)

- Error in memory translator hub
- Recall of around 1 Mio. motherboards
- \$ 253 Mio. financial loss

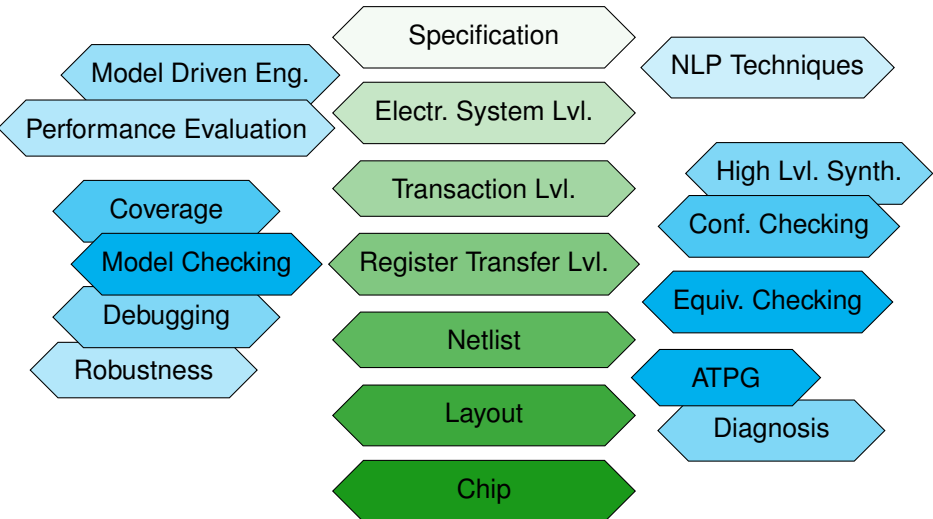
AMD Stack Pointer Bug (2012)

- Specific instruction sequence causes wrong stack pointer update
- Found by linux developer and reproduced on 48 core system

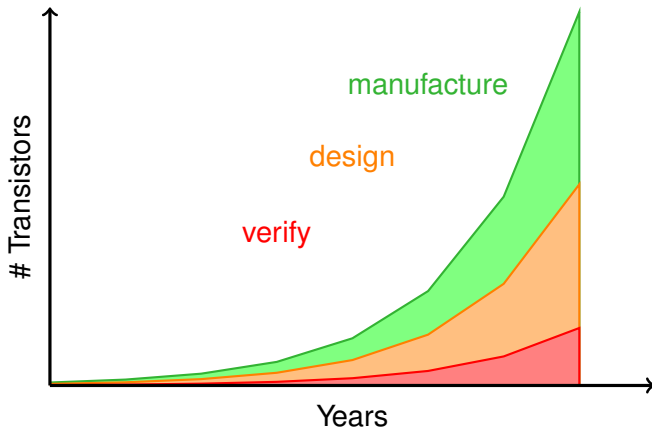
Levels of Abstraction



Quality Assurance



Design Gap – Verification Gap





Outline

Functional Verification

- Circuit Models
- Temporal Logic
- CTL Model Checking
- Bounded Model Checking

Decision Procedures

- Boolean Satisfiability
- Tseitin Transformation
- SAT Solving

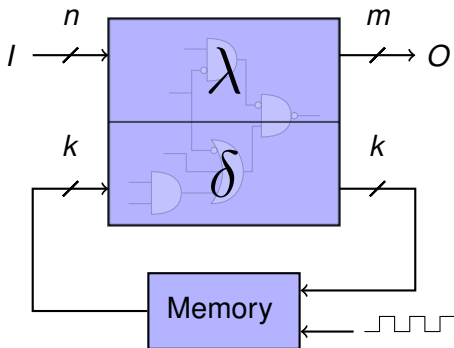
Practical Exercise

- System Verilog Assertions
- Round-Robin Arbiter

Functional Verification

- **Dynamic verification** (= simulation) still standard technology
- Pentium 4 overall simulated cycles < one minute at operation speed [Bentley, 2005]
- Full coverage is **infeasible**
- Increasing use of **formal methods**

Sequential Circuit Model



Mealy Machine:

$$\mathcal{M} = (I, O, S, S_0, \delta, \lambda)$$

$$\delta : S \times I \rightarrow S$$

$$\lambda : S \times I \rightarrow O$$

$$S_0 \subseteq S$$

$$I = \{0, 1\}^n$$

$$O = \{0, 1\}^m$$

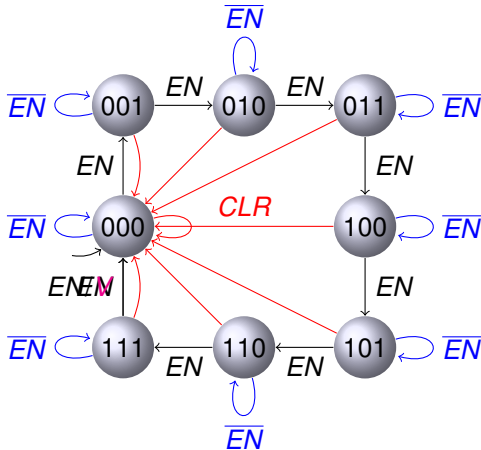
$$S = \{0, 1\}^k$$

```
module count(CLK, EN, CLR,
            S0, S1, S2, V);
```

```
input      CLK, EN, CLR;
output reg S0, S1, S2;
output     V;
```

```
assign V = S0 & S1 & S2 &
          !CLR & EN;
```

```
always @(posedge CLK) begin
    if (CLR) begin
        {S2, S1, S0} <= 0;
    end else begin
        if (EN) begin
            {S2, S1, S0}
            <= {S2, S1, S0} + 1;
        end
    end
end
endmodule // count
```



Verification Model

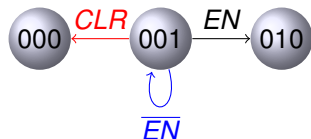
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$$\mathcal{M} = (I, O, S, S_0, \delta, \lambda)$$

$$\delta : S \times I \rightarrow S$$

$$\lambda : S \times I \rightarrow O$$

$$S_0 \subseteq S$$



Kripke Structure:

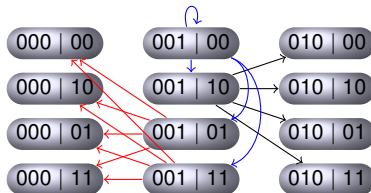
$$\mathcal{K} = (S, S_0, \delta, \mathcal{V}, \mathcal{L})$$

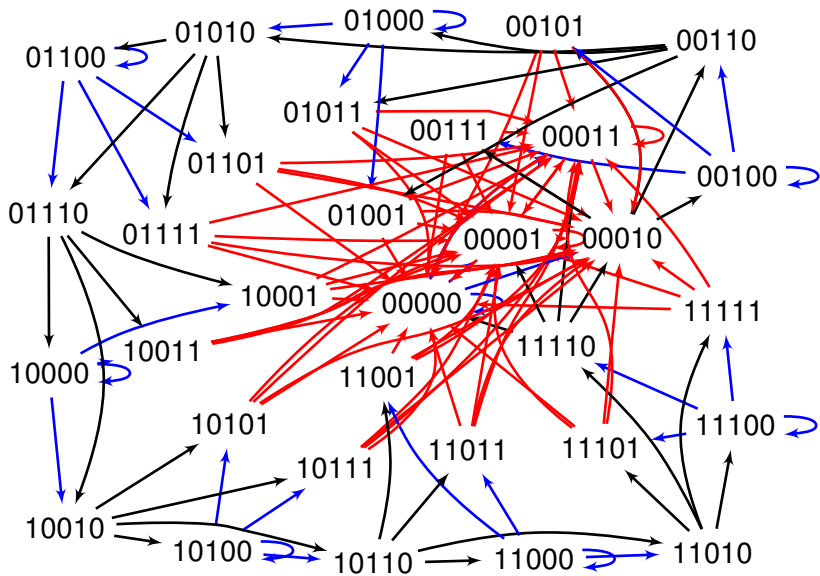
$$\delta \subseteq S \times S \quad \text{transition relation}$$

$$S_0 \subseteq S \quad \text{initial states}$$

$$\mathcal{V} \quad \text{propositional variables}$$

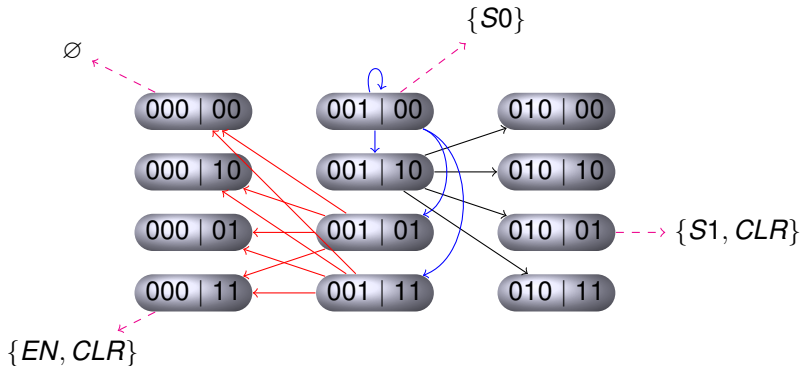
$$\mathcal{L} : S \rightarrow 2^{\mathcal{V}} \quad \text{labelling function}$$





Labelling Function

Propositional variables $\mathcal{V} = \{S2, S1, S0, EN, CLR, V\}$



What do we want to verify?

Safety

Something bad will never happen, e.g.

“The stack pointer will never overflow”

“The traffic lights will never be green at the same time”

Liveness

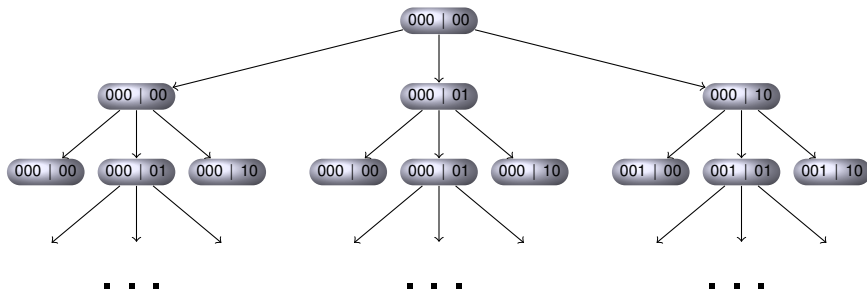
Something good will eventually happen, e.g.

“Every request will be granted”

“The cache and the main memory will eventually be consistent”

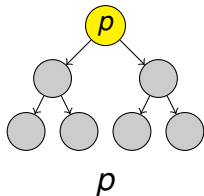
How to specify such properties?

Computation Tree

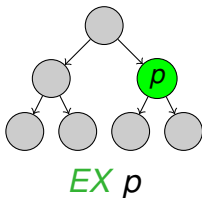


How to specify such properties?

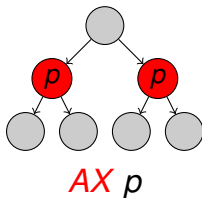
Some property p holds
(in the initial state)



p holds in
some next state



p holds in
all next states

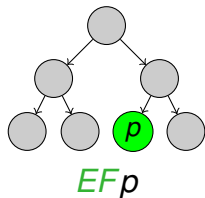


path
quantifier

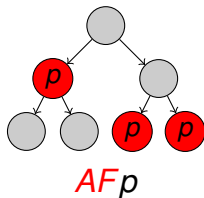
next
operator

Further Modalities

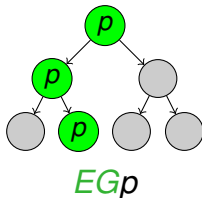
p holds in some future state



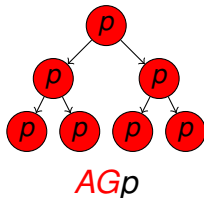
p holds eventually



p holds globally on some path

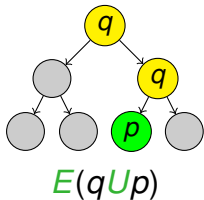


p holds globally on all paths

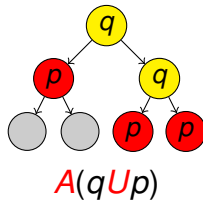


Until Modalities

On some path, q holds until p holds



On all paths, q holds until p holds



Computation Tree Logic

A CTL formula over propositional variables $\mathcal{V}$ has the form

$$\begin{array}{lcl} CTL ::= & p, & \text{where } p \in \mathcal{V} \\ & \varphi \wedge \psi & \neg \varphi \\ & \text{EX } \varphi & \text{AX } \varphi \\ & \text{EF } \varphi & \text{AF } \varphi \\ & \text{EG } \varphi & \text{AG } \varphi \\ & \text{E}(\varphi \text{ U } \psi) & \text{A}(\varphi \text{ U } \psi) \end{array}$$

What do we want to verify?

Safety

“The stack pointer will never overflow” $\text{AG} (\text{sp} < 4096)$

“The traffic lights will never be green at the same time” $\neg \text{EF} (\text{tl}_1 \wedge \text{tl}_2)$

Liveness

“Every request will be granted” $\text{AG} (\text{req} \rightarrow \text{AF gnt})$

“The cache and the main memory will eventually be consistent” $\text{AF} (\text{mem}_i = \text{cache}_i)$

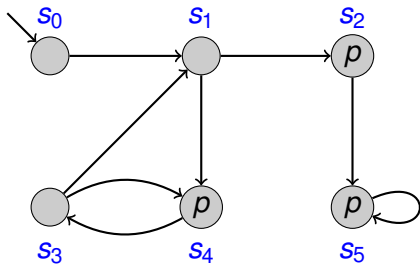
Model Checking

Given a Kripke Structure $\mathcal{K}$ and a CTL formula φ ,
check if $\mathcal{K} \models \varphi$.

How do we do this?

1. Compute all states in which φ holds:
 $\tau(\varphi) = \{s \in S \mid \mathcal{K}, s \models \varphi\}$
2. Check if the initial states are a subset of those states:
 $S_0 \setminus \tau(\varphi) = \emptyset$

Example



$$\tau(p) = \{s_2, s_4, s_5\}$$

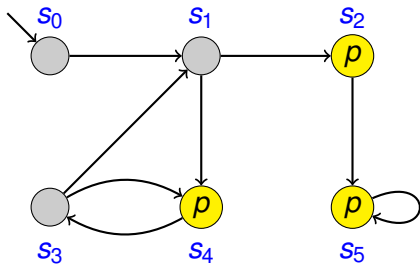
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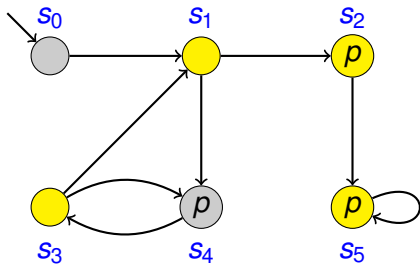
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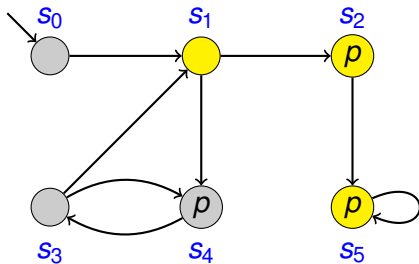
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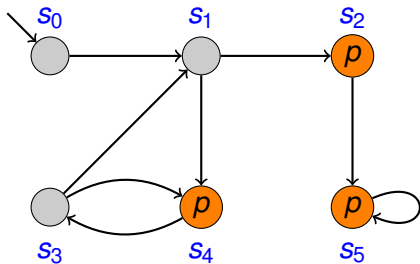
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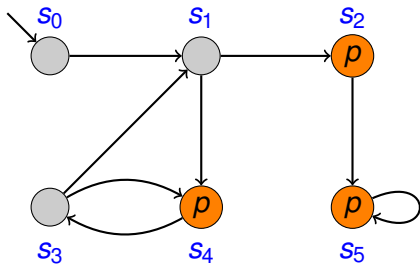
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Example



Expansion rule:

$$\text{EF } \varphi = \varphi \vee \text{EX EF } \varphi$$

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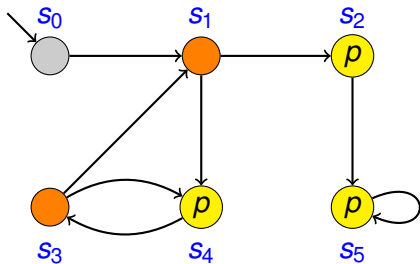
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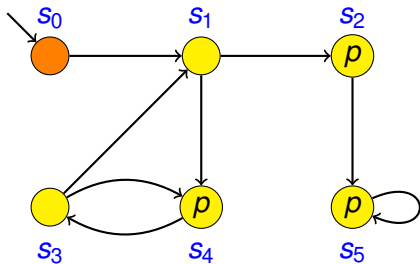
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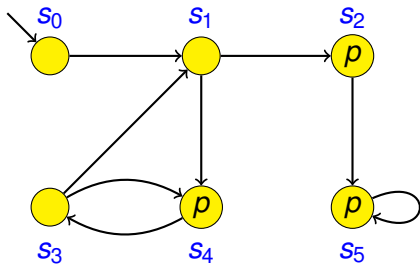
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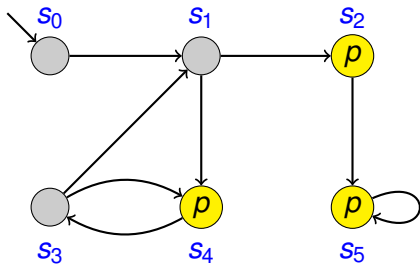
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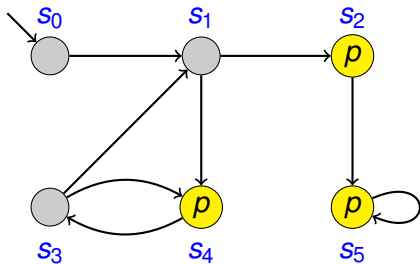
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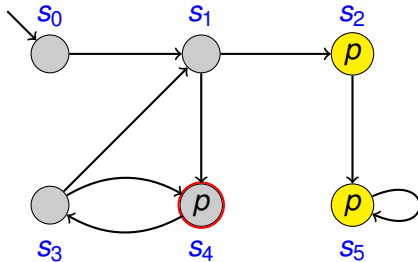
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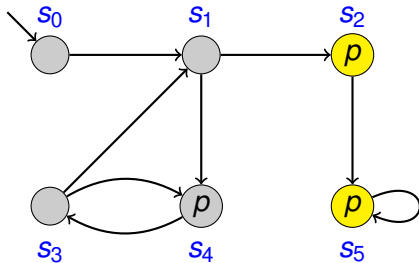
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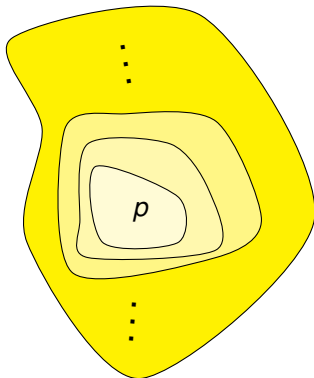
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Fixed Point Algorithm for $\text{EF } p$



$$S_0 = p$$

$$S_1 = p \cup \text{EX } p$$

$$S_2 = p \cup \text{EX } p \cup \text{EX EX } p$$

...

$$S_n = p \cup \bigcup_{i=1}^n \text{EX}^i p = S_{n-1}$$

$$\Rightarrow S_n = \tau(\text{EF } p)$$

Fixed Points

Let $f : \mathcal{P}(S) \rightarrow \mathcal{P}(S)$ a set-valued function and $Z \subseteq G$.

- Z is called a **fixed point** of f if $f(Z) = Z$
- Z is the **least fixed point** of f if it is a fixed point and for all other fixed points U of f it holds that $Z \subseteq U$.
- Z is the **greatest fixed point** of f if it is a fixed point and for all other fixed points U of f it holds that $U \subseteq Z$.

Fixed Points (2)

A function $f : \mathcal{P}(S) \rightarrow \mathcal{P}(S)$ is called **monotone** if for all $X, Y \subseteq S$

$$X \subseteq Y \Rightarrow f(X) \subseteq f(Y) \quad (1)$$

Knaster-Tarski Theorem

Let $f : \mathcal{P}(S) \rightarrow \mathcal{P}(S)$ be a monotone function. Then f has a least and a greatest fixed point.

- $\bigcup_{n \geq 1} f^n(\emptyset)$ is the least fixed point of f .
- $\bigcap_{n \geq 1} f^n(S)$ is the greatest fixed point of f .

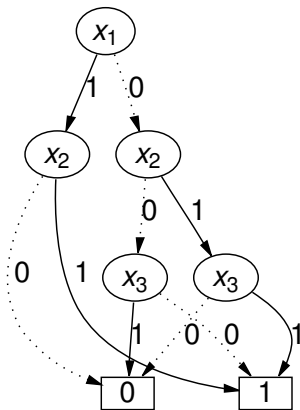
CTL Model Checking

Let $\mathcal{K} = (\mathcal{S}, \mathcal{S}_0, \delta, \mathcal{V}, \mathcal{L})$ be a Kripke structure.

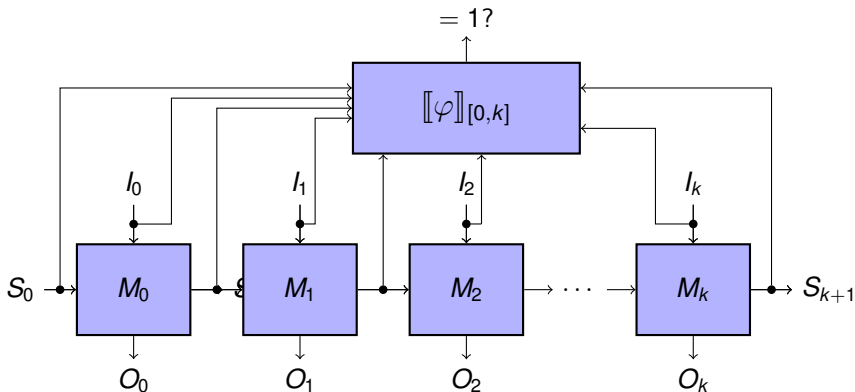
$$\begin{aligned}\tau(p) &= \{s \in \mathcal{S} \mid p \in \mathcal{L}(s)\} \\ \tau(\varphi \wedge \psi) &= \tau(\varphi) \cap \tau(\psi) \\ \tau(\varphi \vee \psi) &= \tau(\varphi) \cup \tau(\psi) \\ \tau(\neg\varphi) &= \mathcal{S} \setminus \tau(\varphi) \\ \tau(\text{EF } \varphi) &= \text{lfp } Z. \tau(\varphi) \cup \text{EX } (Z) \\ \tau(\text{AF } \varphi) &= \text{lfp } Z. \tau(\varphi) \cup \text{AX } (Z) \\ \tau(\text{EG } \varphi) &= \text{gfp } Z. \tau(\varphi) \cap \text{EX } (Z) \\ \tau(\text{AG } \varphi) &= \text{gfp } Z. \tau(\varphi) \cap \text{AX } (Z) \\ \tau(\text{E}(\varphi \text{ U } \psi)) &= \text{lfp } Z. \tau(\psi) \cup (\tau(\varphi) \cap \text{EX } (Z)) \\ \tau(\text{A}(\varphi \text{ U } \psi)) &= \text{lfp } Z. \tau(\psi) \cup (\tau(\varphi) \cap \text{AX } (Z))\end{aligned}$$

Symbolic Model Checking

- Complexity of CTL model checking depending on state space
- Use of **symbolic** representations
- Binary Decision Diagrams (BDDs)
- **State space explosion** still a problem
- Works for small (or very regular) systems
- Popular tool: NuSMV
[Cimatti et al., 2002]

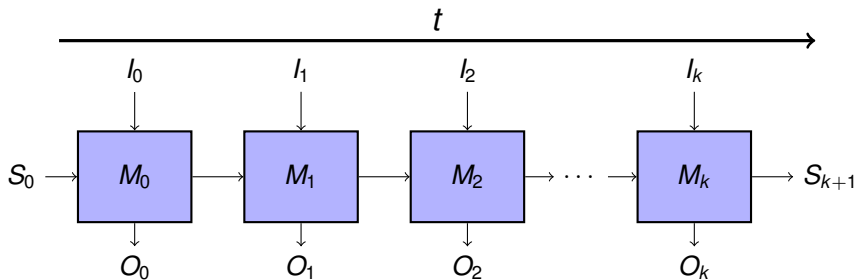


Bounded Model Checking



Bounded Model Checking

- Avoid reachability computation by **unrolling**
- Encode bounded property
- Works well for **safety checking**
- Original method is **incomplete** (bug hunting only)
- Alternatively, use **temporal induction**



Advancements in Model Checking

- Symbolic model checking with BDDs
[Burch et al., 1992]
- SAT-based bounded model checking
[Biere et al., 1999]
- Counter-example guided abstraction
refinement [Clarke et al., 2003]
- Inductive invariant checking
[Bradley, 2011]

μ , *CTL*, *LTL*

LTL, *ACTL*

AG p



Outline

Functional Verification

Circuit Models

Temporal Logic

CTL Model Checking

Bounded Model Checking

Decision Procedures

Boolean Satisfiability

Tseitin Transformation

SAT Solving

Practical Exercise

System Verilog Assertions

Round-Robin Arbiter

Boolean Satisfiability (SAT)

SAT Problem

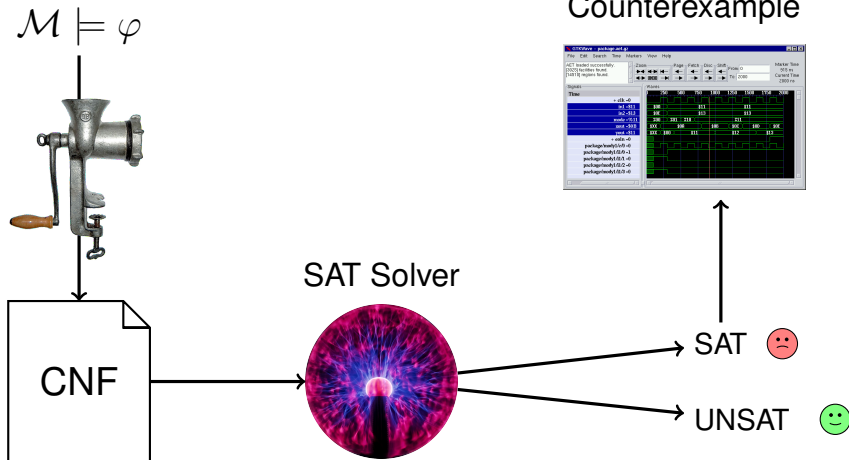
Given a Boolean function $f : \{0, 1\}^n \rightarrow \{0, 1\}$ (in conjunctive normal form), is there an assignment $X \in \{0, 1\}^n$, such that $f(X) = 1$?

Conjunctive Normal Form

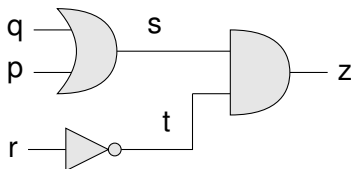
A Boolean formula over variables $X = \{x_0 \dots x_n\}$ is in conjunctive normal form if it is a **conjunction of clauses** $(\ell_{1,1} \vee \ell_{1,2} \vee \dots \vee \ell_{1,m_0}) \wedge \dots \wedge (\ell_{k,1} \vee \dots \vee \ell_{k,m_k})$. A clause is a **disjunction of literals** $\ell = x_i$ or $\ell = \neg x_i$ for some $x_i \in X$.

- NP-complete problem [Cook, 1971]

SAT-Based BMC



Tseitin Transformation



$$z \leftrightarrow (p \vee q) \wedge \neg r$$

$$s \leftrightarrow p \vee q$$

$$t \leftrightarrow \neg r$$

$$z \leftrightarrow s \wedge t$$

$$\begin{aligned} s \leftrightarrow p \vee q &\equiv (s \rightarrow p \vee q) \wedge (p \vee q \rightarrow s) \\ &\equiv (\neg s \vee p \vee q) \wedge (\neg(p \vee q) \vee s) \\ &\equiv (\neg s \vee p \vee q) \wedge ((\neg p \wedge \neg q) \vee s) \\ &\equiv (\neg s \vee p \vee q) \wedge (\neg p \vee s) \wedge (\neg q \vee s) \end{aligned}$$

$$t \leftrightarrow \neg r \equiv (\neg t \vee \neg r) \wedge (t \vee r)$$

$$z \leftrightarrow s \wedge t \equiv (\neg s \vee \neg t \vee z) \wedge (s \vee \neg z) \wedge (t \vee \neg z)$$

How it Looks Like in Practice...

c example circuit

c

p cnf 6 8

-4 1 2 0 $\leftarrow (\neg s \vee p \vee q) \wedge$

-1 4 0 $\leftarrow (\neg p \vee s) \wedge$

-2 4 0 $\leftarrow (\neg q \vee s) \wedge$

-5 -3 0 $\leftarrow (\neg t \vee \neg r) \wedge \dots$

5 3 0

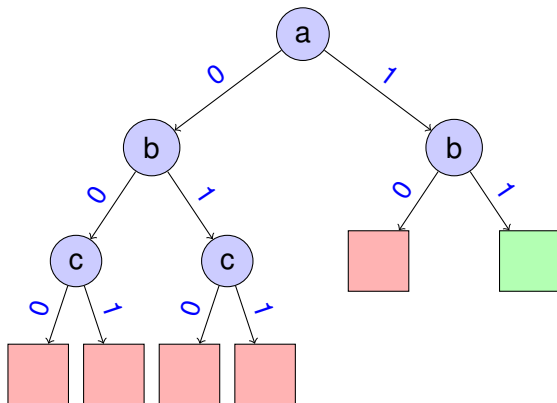
-4 -3 6 0

4 -6 0

5 -6 0

SAT Solving in a Nutshell

$(\neg a \vee b \vee c)$
 $(a \vee c \vee d)$
 $(a \vee c \vee \neg d)$
 $(a \vee \neg c \vee d)$
 $(a \vee \neg c \vee \neg d)$
 $(\neg b \vee \neg c \vee d)$
 $(\neg a \vee b \vee \neg c)$
 $(\neg a \vee \neg b \vee c)$



Advancements in SAT Solving

- **1962:** DPLL backtracking algorithm [Davis et al., 1962]
- **1996:** Conflict learning [Silva and Sakallah, 1996]
- **2001:** Local search, decision heuristics, engineering ...
- Modern solvers handle **millions** of variables and clauses
- Popular solvers:
 - MiniSAT
 - Glucose
 - Lingeling
- Extensions of SAT:
 - Satisfiability Modulo Theories (SMT)
 - Quantified Boolean Formulae (QBF)
 - Max-SAT

Summary Decision Procedures

- Separation of **verification problem** and **decision engine**
- Many many applications in hardware & software verification
- Convenient and **standardized APIs** for ease of use
- Active field of research
- Popular SMT solvers:
 - MathSAT
 - Z3 (Microsoft Research)
 - STP (Stanford)
 - Yices



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Practical Exercise

- System Verilog Assertions
- Round-Robin Arbiter

System Verilog Assertions (Reminder)

```
module monitor( foo.MONITOR I );

    property slave_data_notunknown_when_ready;
        @(posedge I.clk)
            I.ready | -> $isunknown(I.s) == 0;
    endproperty

    assert_slave_data_notunknown_when_ready: assert property (slave_data_notunknown_when_ready)
        else $error("%m: ready is asserted but data from slave is non valid");

    property slave_ready_until_valid;
        @(posedge I.clk)
            $rose(I.ready) | -> I.ready throughout I.valid [->1]; //ou I.ready [*0:$] ##1 I.valid;
    endproperty

    assert_slave_ready_until_valid: assert property(slave_ready_until_valid)
        else $error("%m:slave's ready must be held until valid is set");

    property slave_data_held_when_ready;
        bit [7:0] s;
        @(posedge I.clk) disable iff (I.nrst == 0)
            (I.ready && !I.valid , s = I.s) | => s == I.s; //ou $stable(I.s);
    endproperty

    assert_slave_data_held_when_ready: assert property(slave_data_held_when_ready)
        else $error("%m: data must be held stable when slave is ready");
endmodule
```

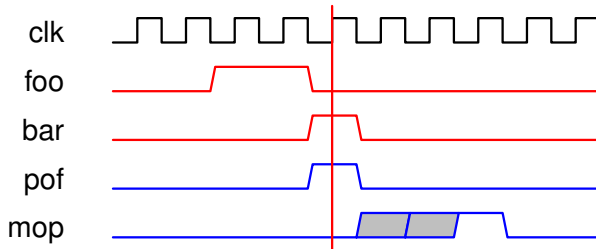
Basic Property Structure

```
// basic property structure
property foo;
    @(posedge clk) disable iff (rst)
        expr;
endproperty // foo

// verification directives
assert_foo: assert property(foo);
assume_foo: assume property(foo);
```

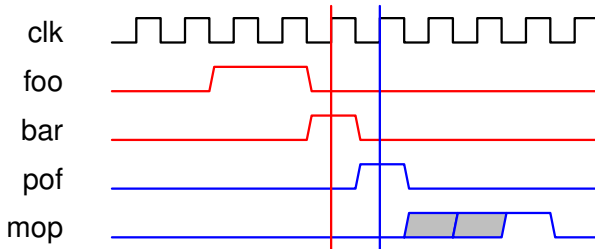

Sequences and Suffix Implication

```
// suffix implication  
foo ## bar |-> pof ##[1:3] mop;
```



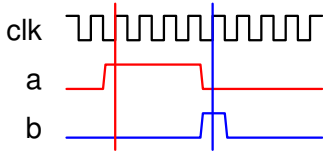
Non-Overlapping Suffix Implication

```
// non-overlapping suffix implication  
foo ## bar | => pof ##[1:3] mop;
```

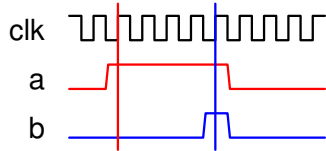


Until

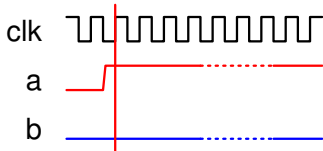
a until b
a s_until b



a until_with b
a s_until_with b

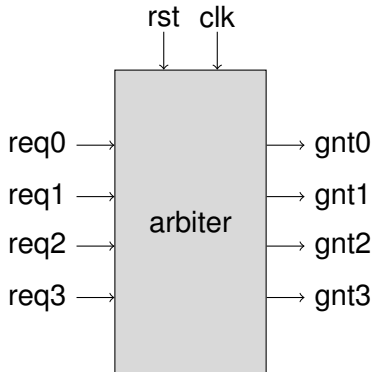


a until b
a until_with b



- Overlapping vs. non-overlapping
- Weak vs. strong

Round-Robin Arbiter



- Arbitration of four masters
- Single request always granted
- Fair arbitration of multiple (simultaneous) requests



Practical Exercise

Let's get to work. . .

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