



Formal Verification

SE303 – Conception des
systèmes sur puces (SoC)

Ulrich Kühne
29/11/2017





Outline

Introduction

- Short History of Hardware Failures
- Design and Verification Process

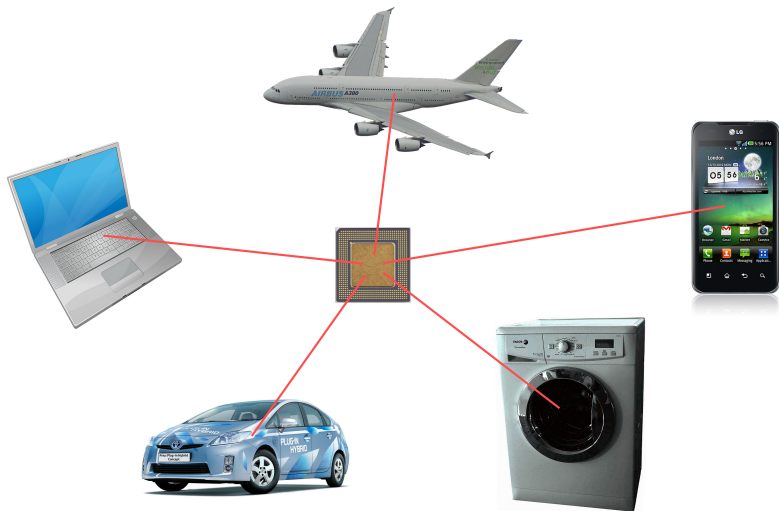
Functional Verification

- Circuit Models
- Linear Time Logic (LTL)
- Computation Tree Logic (CTL)
- Model Checking

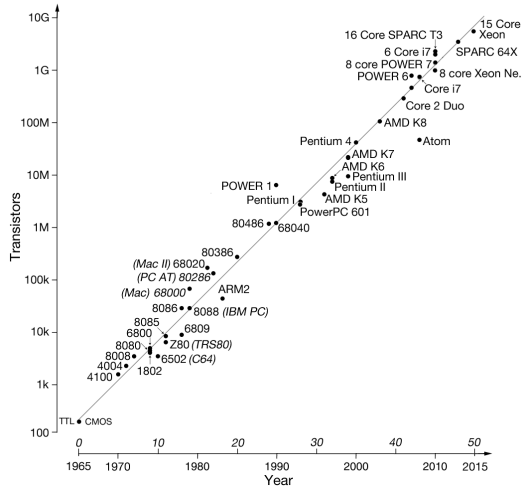
Equivalence Checking

- Problem Formulation
- Boolean Satisfiability

Motivation

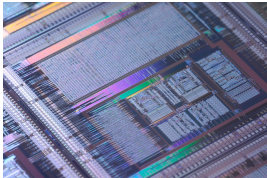


Motivation



[Source: www.elektormagazine.com/articles/moores-law]

Motivation



[© photo by mark.sze]

- Transistor count of **> 3 billion**
- Gate level models are **huge**
- Big designer teams (several hundreds)
- Big **correctness** issues
- Late bugs are extremely expensive

Motivation

The First Bug (1947)

9/9

0800 Antan started
1000 " stopped - antan ✓
1300 (032) MP-MC 1.58266000
033 PRO 2 2.130476415
correct 2.130676415
Relays 6-2 in 033 failed special speed test
in relay 11,000 test.
Relays changed
1100 Started Cosine Tapc (Sine check)
1525 Started Multy Adder Test.
1545 Relay #70 Panel F
(moth) in relay.
First actual case of bug being found.
1630 Antan started.
1700 closed down.

Relay 3145
Relay 3370

[Photo: U.S. Naval Historical Center]

Motivation

The Pentium FDIV Bug (1994)

$$\text{let } x = 4195835, y = 3145727 \Rightarrow x - \frac{x}{y} \cdot y = 256$$

- Bug in floating point unit $\Rightarrow$ \$ 450 Mio. loss for Intel

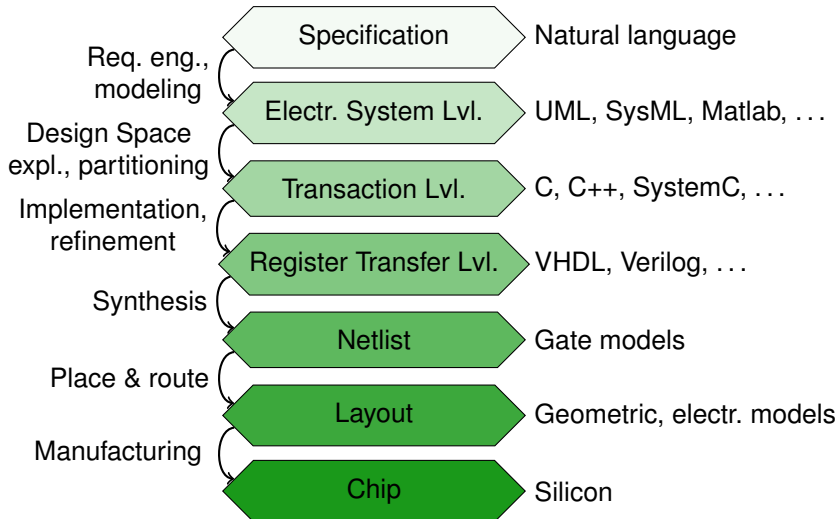
820 Chipset MTH Bug (2000)

- Error in memory translator hub
- Recall of around 1 Mio. motherboards
- \$ 253 Mio. financial loss

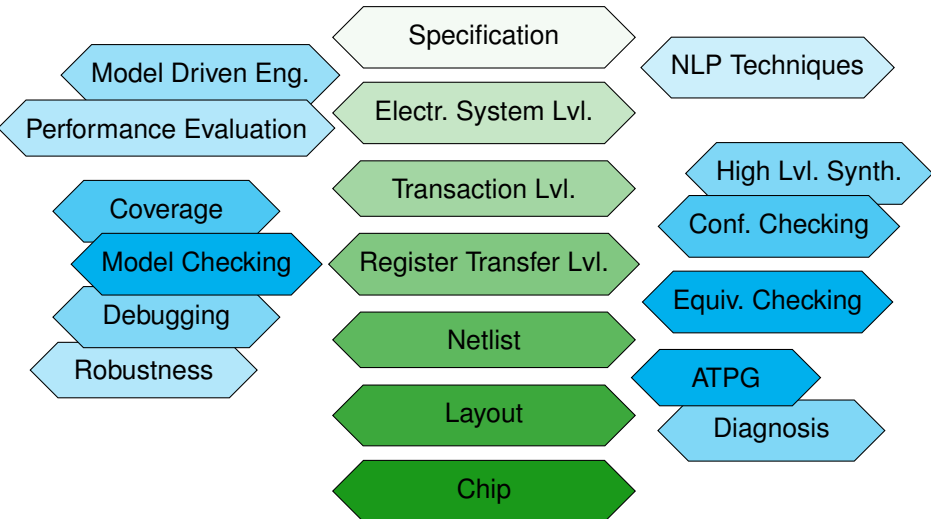
Intel i6/i7 (Skylake) Hyperthreading Bug (2017)

- Specific operating conditions cause unpredictable behavior
- Found by Linux/OCaml developers

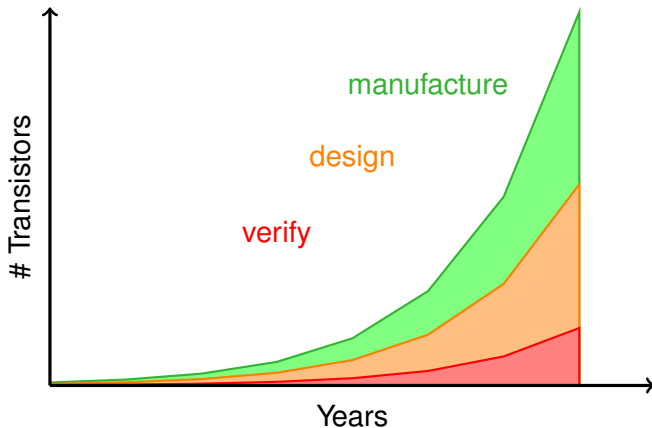
Hardware Design Flow



Hardware Verification Flow



Design Gap – Verification Gap





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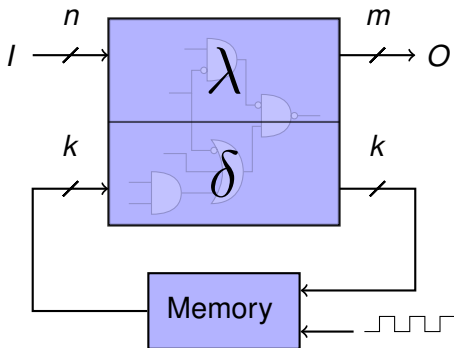
Equivalence Checking

Problem Formulation
Boolean Satisfiability

Functional Verification

- **Dynamic verification** (= simulation)
still standard technology
- Pentium 4 overall simulated cycles < one minute
at operation speed [Bentley, 2005]
- Full coverage is **infeasible**
- Increasing use of **formal methods**

Sequential Circuit Model



Mealy Machine:

$$\mathcal{M} = (I, O, S, S_0, \delta, \lambda)$$

$$\delta : S \times I \rightarrow S$$

$$\lambda : S \times I \rightarrow O$$

$$S_0 \subseteq S$$

$$I = \{0, 1\}^n$$

$$O = \{0, 1\}^m$$

$$S = \{0, 1\}^k$$

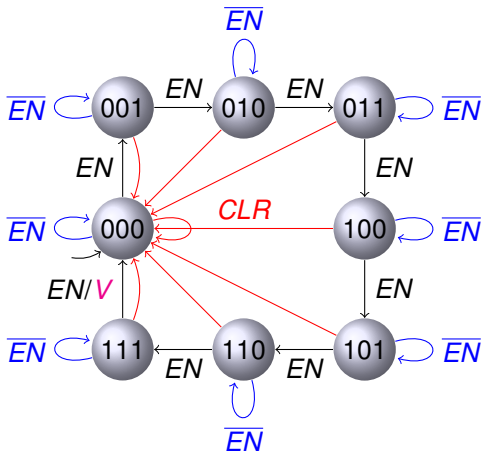
From Verilog to Mealy Machine

```
module count(CLK, EN, CLR,  
            S0, S1, S2, V);
```

```
input  CLK, EN, CLR;  
output reg S0, S1, S2;  
output  V;
```

```
assign V = S0 & S1 & S2 &  
        !CLR & EN;
```

```
always @(posedge CLK) begin  
  if (CLR)  
    {S2, S1, S0} <= 0;  
  else if (EN)  
    {S2, S1, S0}  
    <= {S2, S1, S0} + 1;  
end  
endmodule // count
```



What do we want to verify?

Safety

Something bad will never happen, e.g.

“The stack pointer will never overflow”

“The traffic lights will never be green at the same time”

Liveness

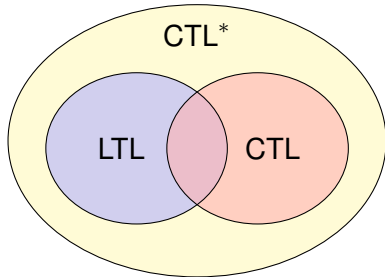
Something good will eventually happen, e.g.

“Every request will be granted”

“The cache and the main memory will eventually be consistent”

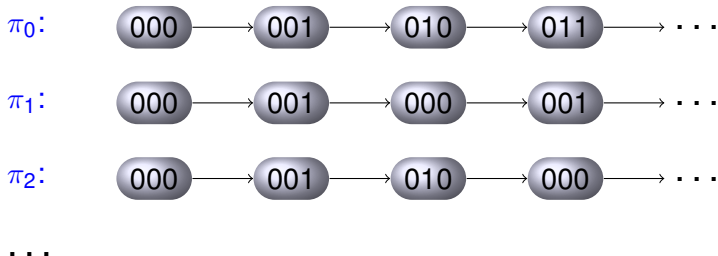
How to specify such properties?

- Temporal logic = propositional logic + time
- Discrete vs. continuous time
- Linear time view
- Branching time view

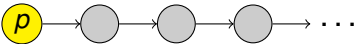
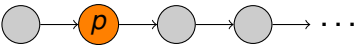
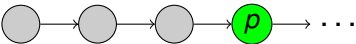


The Linear Time View

Computation paths



Linear Time Logic (LTL)

p holds (in the initial state)		p
p holds in the next state		Xp
p holds in the future		Fp
p holds globally		Gp
p holds until q		$p \text{ U } q$

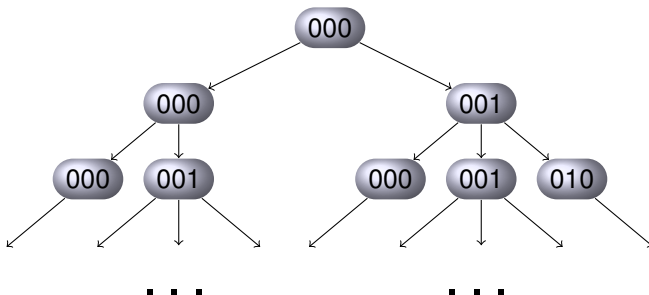
Linear Time Logic (LTL)

An LTL formula over propositional variables $\mathcal{V}$ has the form

$$\begin{array}{lcl} LTL ::= & p, & \text{where } p \in \mathcal{V} \\ & \neg \varphi \\ & \varphi \wedge \psi \\ & \mathbf{X} \varphi \\ & \mathbf{F} \varphi \\ & \mathbf{G} \varphi \\ & \varphi \mathbf{U} \psi, & \text{where } \varphi, \psi \in LTL. \end{array}$$

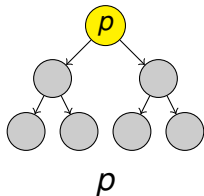
Branching Time View

Computation Tree

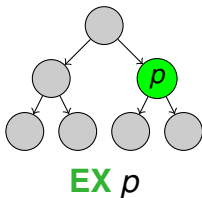


Computation Tree Logic (CTL)

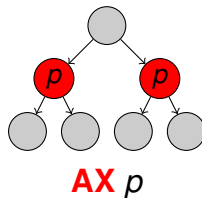
Some property p holds
(in the initial state)



p holds in
some next state



p holds in
all next states

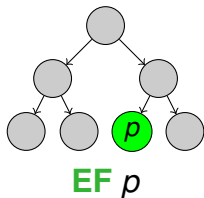


path
quantifier

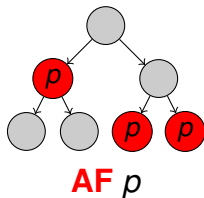
next
operator

Further Modalities

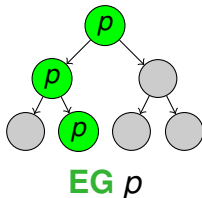
p holds in some future state



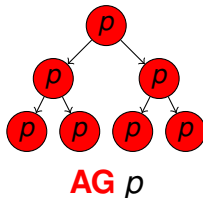
p holds eventually



p holds globally on some path

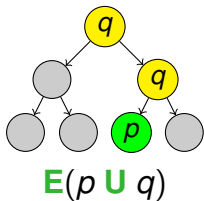


p holds globally on all paths

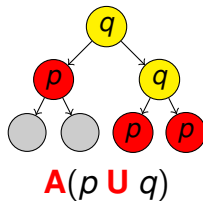


Until Modalities

On some path, q holds
until p holds



On all paths, q holds
until p holds



Computation Tree Logic (CTL)

A CTL formula over propositional variables $\mathcal{V}$ has the form

$$\begin{array}{lcl} CTL ::= & p, & \text{where } p \in \mathcal{V} \\ & \varphi \wedge \psi & \neg \varphi \\ & \mathbf{EX} \varphi & \mathbf{AX} \varphi \\ & \mathbf{EF} \varphi & \mathbf{AF} \varphi \\ & \mathbf{EG} \varphi & \mathbf{AG} \varphi \\ & \mathbf{E}(\varphi \mathbf{U} \psi) & \mathbf{A}(\varphi \mathbf{U} \psi), \text{ where } \varphi, \psi \in CTL \end{array}$$

What do we want to verify?

Safety

“The stack pointer will never overflow” **AG** ($sp < 4096$)

“The traffic lights will never be green at the same time” $\neg$ **EF** ($tl_1 \wedge tl_2$)

Liveness

“Every request will be granted” **AG** ($req \rightarrow$ **AF** gnt)

“The cache and the main memory will eventually be consistent” **AF** ($mem_i = cache_i$)

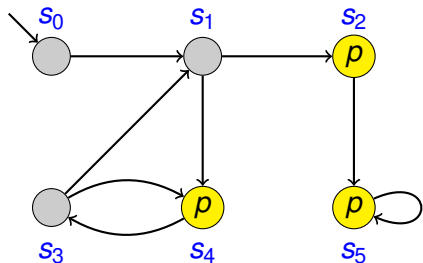
Model Checking

Given a Mealy Machine $\mathcal{M}$ and a CTL formula φ ,
check if $\mathcal{M} \models \varphi$.

How do we do this?

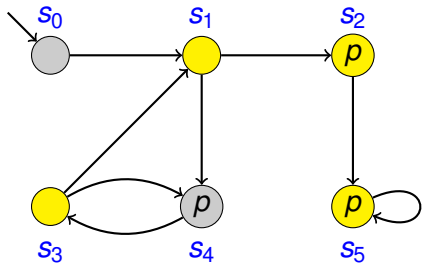
1. Compute all states in which φ holds:
$$\tau(\varphi) = \{s \in S \mid \mathcal{M}, s \models \varphi\}$$
2. Check if the initial states are a subset of those states:
$$S_0 \setminus \tau(\varphi) = \emptyset$$

Example



$$\tau(p) = \{s_2, s_4, s_5\}$$

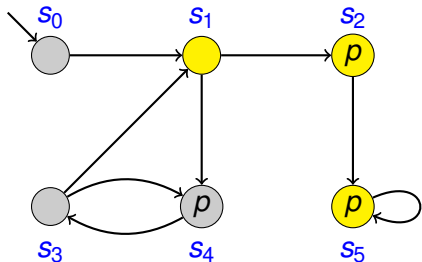
Example



$$\tau(p) = \{s_2, s_4, s_5\}$$

$$\tau(\text{EX } p) = \{s_1, s_2, s_3, s_5\}$$

Example

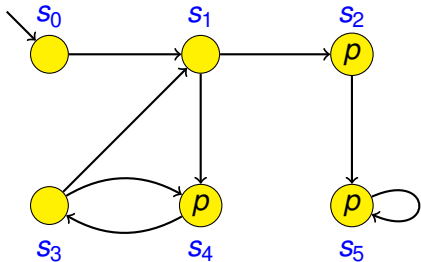


$$\tau(p) = \{s_2, s_4, s_5\}$$

$$\tau(\text{EX } p) = \{s_1, s_2, s_3, s_5\}$$

$$\tau(\text{AX } p) = \{s_1, s_2, s_5\}$$

Example



$$\tau(p) = \{s_2, s_4, s_5\}$$

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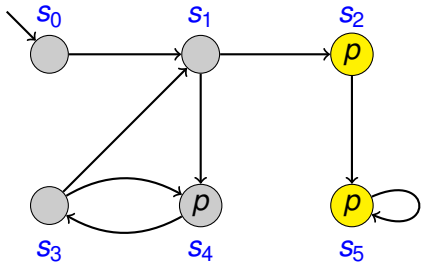
$$\tau(\text{AX } p) = \{s_1, s_2, s_5\}$$

$$\tau(\text{EF } p) = \{s_2, s_4, s_5\} \\ \cup \{s_1, s_3\} \cup \{s_0\}$$

Expansion rules:

$$\text{EF } \varphi = \varphi \vee \text{EX EF } \varphi$$

Example



$$\tau(p) = \{s_2, s_4, s_5\}$$

$$\tau(\text{EX } p) = \{s_1, s_2, s_3, s_5\}$$

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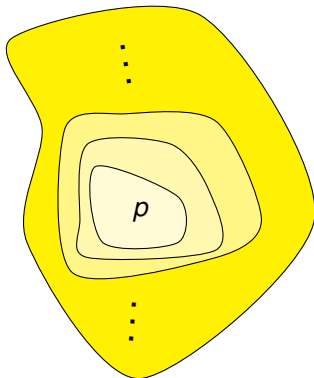
Expansion rules:

$$\text{EF } \varphi = \varphi \vee \text{EX EF } \varphi$$

$$\text{AG } \varphi = \varphi \wedge \text{AX AG } \varphi$$

$$\tau(\text{AG } p) = \{s_2, s_4, s_5\} \cap \{s_2, s_5\}$$

Fixed Point Algorithm for **EF** p



$$S_0 = p$$

$$S_1 = p \cup \mathbf{EX} p$$

$$S_2 = p \cup \mathbf{EX} p \cup \mathbf{EX EX} p$$

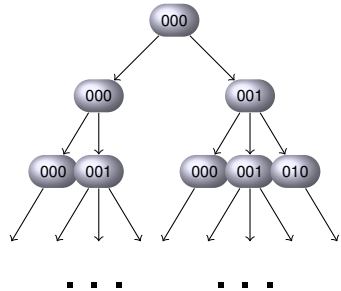
$\dots$

$$S_n = p \cup \bigcup_{i=1}^n \mathbf{EX}^i p = S_{n-1}$$

$$\Rightarrow S_n = \tau(\mathbf{EF} p)$$

Model Checking

- Complexity depends heavily on state space
- Need for efficient data structures
- **State space explosion** still a problem
- Works for small to medium (or very regular) systems
- Popular tool: NuSMV
[Cimatti et al., 2002]
- Ongoing research





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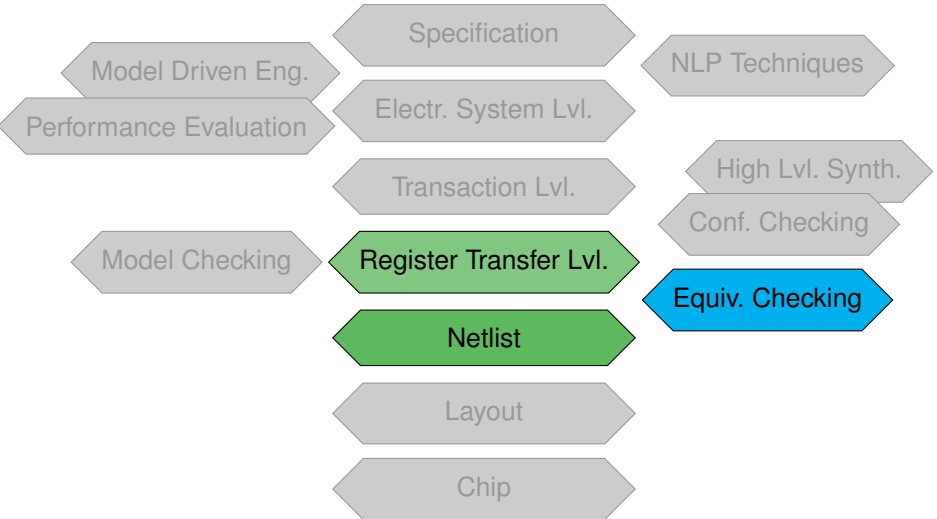
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Equivalence Checking

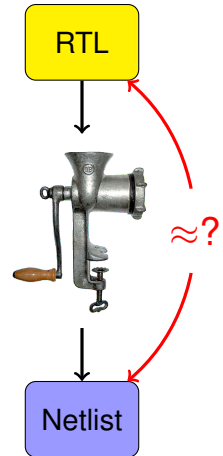
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Equivalence Checking

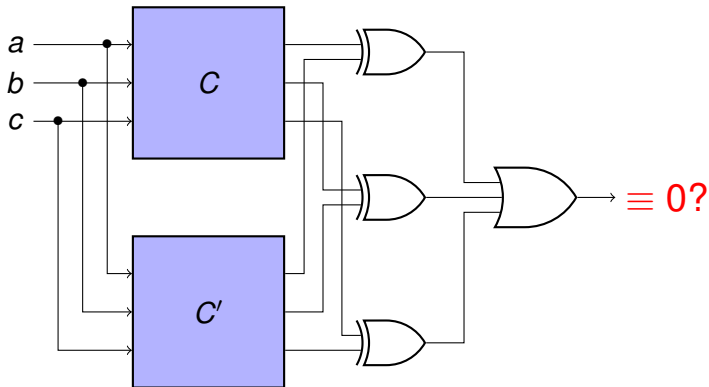


Equivalence Checking

- Hardware *synthesis* is complex
- Aggressive *optimization*
- Automatic pipelining, retiming, ...
- Technology mapping
- Tools are closed source
- Does the netlist do what we think it does?



Miter Structure



Boolean Satisfiability (SAT)

SAT Problem

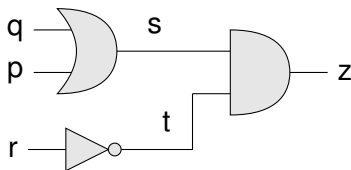
Given a Boolean function $f : \{0, 1\}^n \rightarrow \{0, 1\}$ (in conjunctive normal form), is there an assignment $X \in \{0, 1\}^n$, such that $f(X) = 1$?

Conjunctive Normal Form

A Boolean formula over variables $X = \{x_0 \dots x_n\}$ is in conjunctive normal form if it is a **conjunction of clauses** $(l_{1,1} \vee l_{1,2} \vee \dots \vee l_{1,m_0}) \wedge \dots \wedge (l_{k,1} \vee \dots \vee l_{k,m_k})$. A clause is a **disjunction of literals** $l = x_i$ or $l = \neg x_i$ for some $x_i \in X$.

- NP-complete problem [Cook, 1971]

Tseitin Transformation



$$z \leftrightarrow (p \vee q) \wedge \neg r$$

$$s \leftrightarrow p \vee q$$

$$t \leftrightarrow \neg r$$

$$z \leftrightarrow s \wedge t$$

$$\begin{aligned} s \leftrightarrow p \vee q &\equiv (s \rightarrow p \vee q) \wedge (p \vee q \rightarrow s) \\ &\equiv (\neg s \vee p \vee q) \wedge (\neg(p \vee q) \vee s) \\ &\equiv (\neg s \vee p \vee q) \wedge ((\neg p \wedge \neg q) \vee s) \\ &\equiv (\neg s \vee p \vee q) \wedge (\neg p \vee s) \wedge (\neg q \vee s) \end{aligned}$$

$$t \leftrightarrow \neg r \equiv (\neg t \vee \neg r) \wedge (t \vee r)$$

$$z \leftrightarrow s \wedge t \equiv (\neg s \vee \neg t \vee z) \wedge (s \vee \neg z) \wedge (t \vee \neg z)$$

How it Looks Like in Practice...

c example circuit

c

p cnf 6 8

-4 1 2 0 $\leftarrow (\neg s \vee p \vee q) \wedge$

-1 4 0 $\leftarrow (\neg p \vee s) \wedge$

-2 4 0 $\leftarrow (\neg q \vee s) \wedge$

-5 -3 0 $\leftarrow (\neg t \vee \neg r) \wedge \dots$

5 3 0

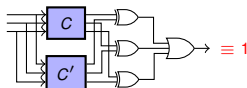
-4 -3 6 0

4 -6 0

5 -6 0

SAT-Based Equivalence Checking

Problem



CNF

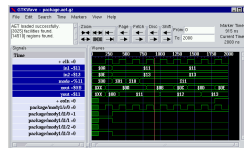
SAT Solver



SAT ☹️

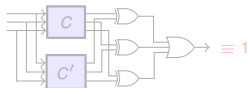
UNSAT 😊

Counterexample

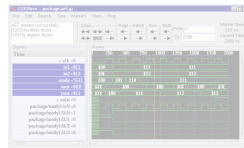


SAT-Based Equivalence Checking

Problem

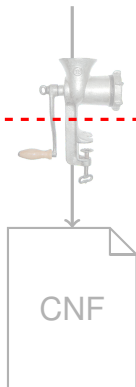


Counterexample

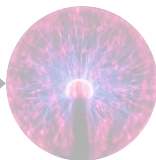


Problem

Encoding



SAT Solver



SAT ☹️

UNSAT 😊

DPLL Algorithm

- Davis-Putnam-Logemann-Loveland [Davis et al., 1962]

DPLL

Data: Set of clauses $\mathcal{C}$

DPLL($\mathcal{C}$) begin

if *all clauses satisfied* **then**

 └ **return** SAT

if $\mathcal{C}$ *contains empty clause* **then**

 └ **return** UNSAT

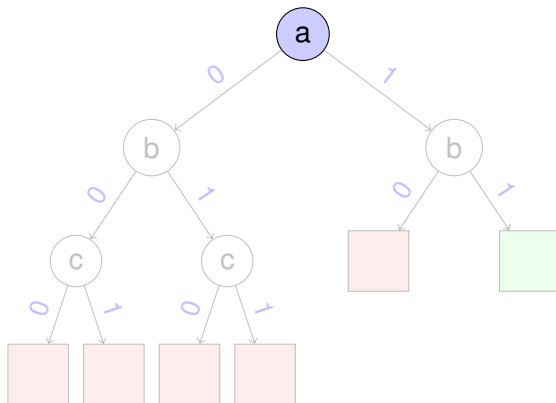
 Propagate();

$\ell \leftarrow \text{ChooseLiteral}();$

 └ **return** DPLL($\mathcal{C} \wedge \ell$) or DPLL($\mathcal{C} \wedge \neg \ell$)

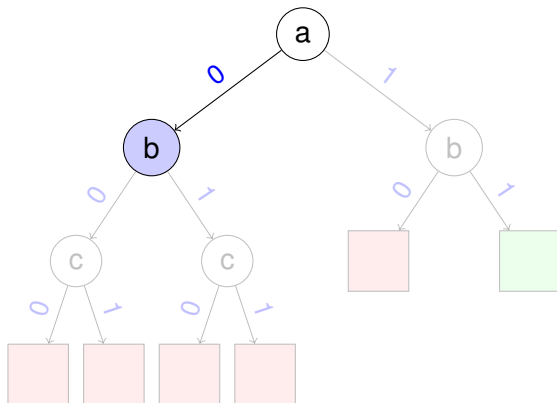
SAT Solving in a Nutshell

$(\neg a \vee b \vee c)$
 $(a \vee c \vee d)$
 $(a \vee c \vee \neg d)$
 $(a \vee \neg c \vee d)$
 $(a \vee \neg c \vee \neg d)$
 $(\neg b \vee \neg c \vee d)$
 $(\neg a \vee b \vee \neg c)$
 $(\neg a \vee \neg b \vee c)$



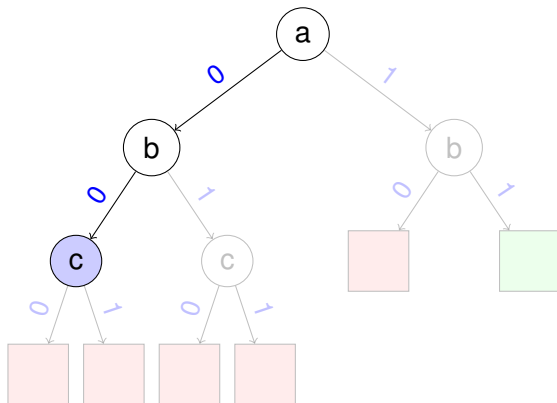
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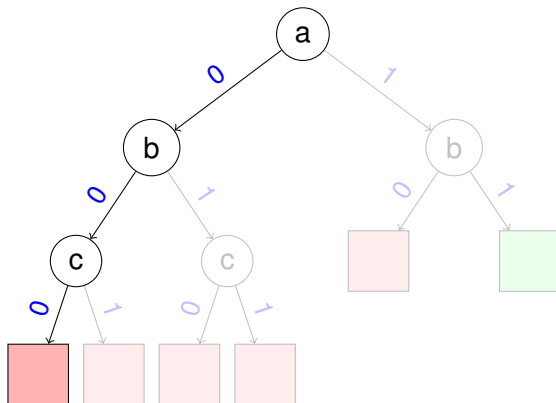
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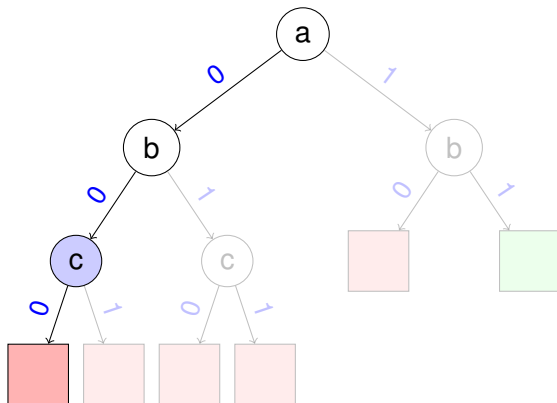
SAT Solving in a Nutshell

$(\neg a \vee b \vee c)$
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 $(a \vee \neg c \vee \neg d)$
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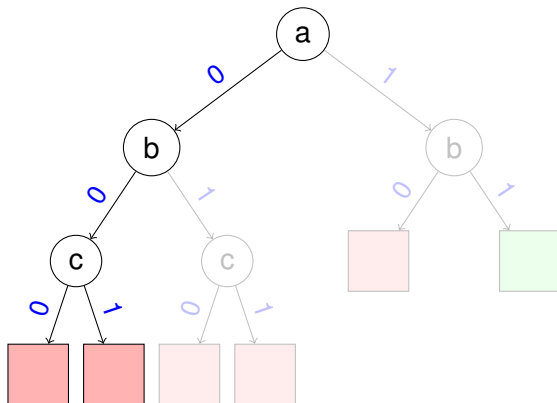
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$(\neg b \vee \neg c \vee d)$
$(\neg a \vee b \vee \neg c)$
$(\neg a \vee \neg b \vee c)$



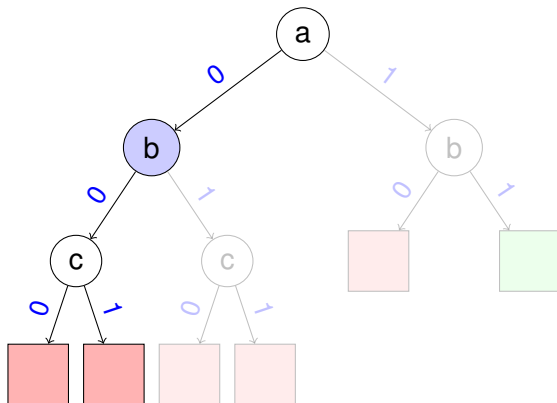
SAT Solving in a Nutshell

$(\neg a \vee b \vee c)$
 $(a \vee c \vee d)$
 $(a \vee c \vee \neg d)$
 $(a \vee \neg c \vee d)$
 $(a \vee \neg c \vee \neg d)$
 $(\neg b \vee \neg c \vee d)$
 $(\neg a \vee b \vee \neg c)$
 $(\neg a \vee \neg b \vee c)$



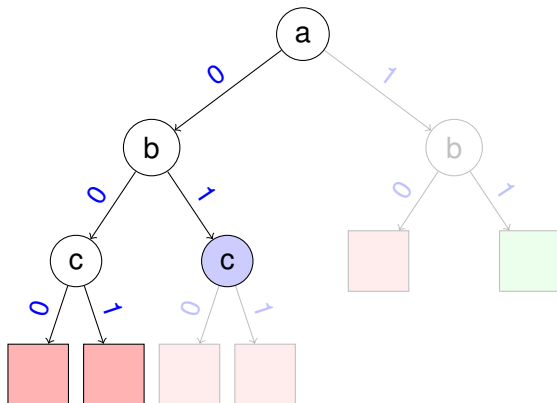
SAT Solving in a Nutshell

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 $(a \vee c \vee d)$
 $(a \vee c \vee \neg d)$
 $(a \vee \neg c \vee d)$
 $(a \vee \neg c \vee \neg d)$
 $(\neg b \vee \neg c \vee d)$
 $(\neg a \vee b \vee \neg c)$
 $(\neg a \vee \neg b \vee c)$



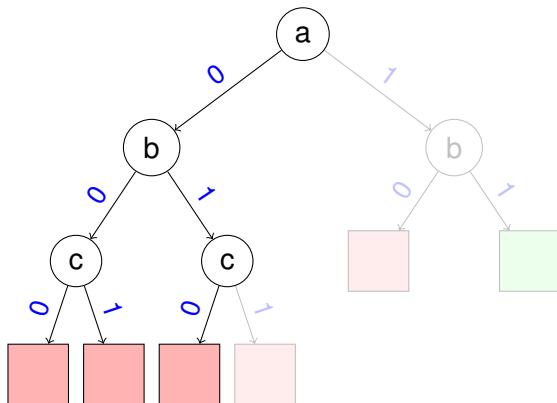
SAT Solving in a Nutshell

$(\neg a \vee b \vee c)$
 $(a \vee c \vee d)$
 $(a \vee c \vee \neg d)$
 $(a \vee \neg c \vee d)$
 $(a \vee \neg c \vee \neg d)$
 $(\neg b \vee \neg c \vee d)$
 $(\neg a \vee b \vee \neg c)$
 $(\neg a \vee \neg b \vee c)$



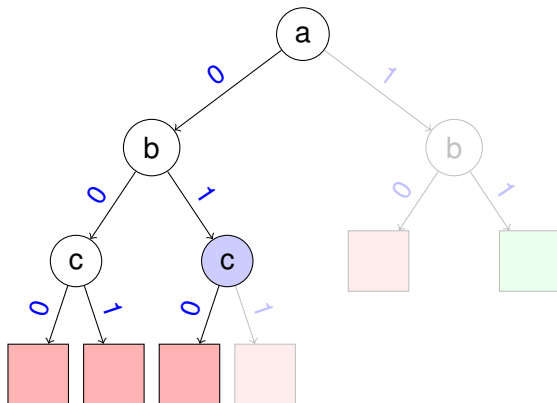
SAT Solving in a Nutshell

$(\neg a \vee b \vee c)$
 $(a \vee c \vee d)$
 $(a \vee c \vee \neg d)$
 $(a \vee \neg c \vee d)$
 $(a \vee \neg c \vee \neg d)$
 $(\neg b \vee \neg c \vee d)$
 $(\neg a \vee b \vee \neg c)$
 $(\neg a \vee \neg b \vee c)$



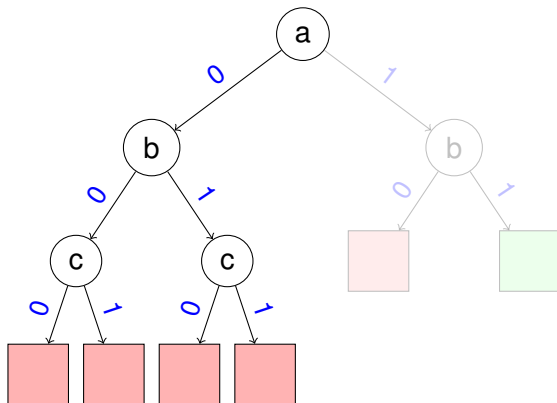
SAT Solving in a Nutshell

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 $(a \vee c \vee \neg d)$
 $(a \vee \neg c \vee d)$
 $(a \vee \neg c \vee \neg d)$
 $(\neg b \vee \neg c \vee d)$
 $(\neg a \vee b \vee \neg c)$
 $(\neg a \vee \neg b \vee c)$



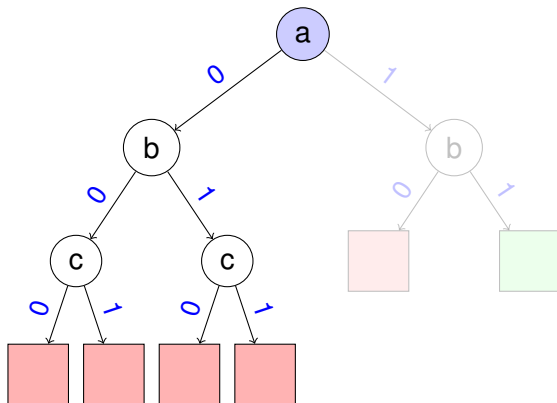
SAT Solving in a Nutshell

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 $(a \vee c \vee \neg d)$
 $(a \vee \neg c \vee d)$
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 $(\neg b \vee \neg c \vee d)$
 $(\neg a \vee b \vee \neg c)$
 $(\neg a \vee \neg b \vee c)$



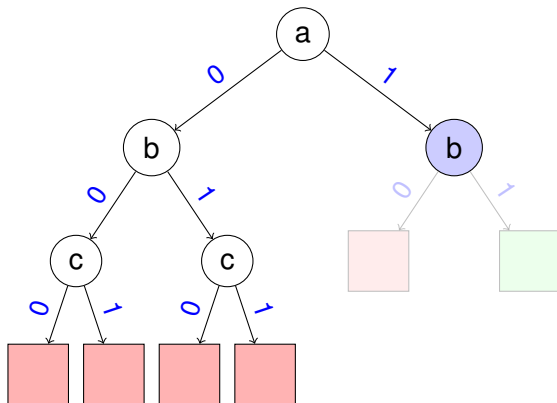
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 $(\neg a \vee \neg b \vee c)$



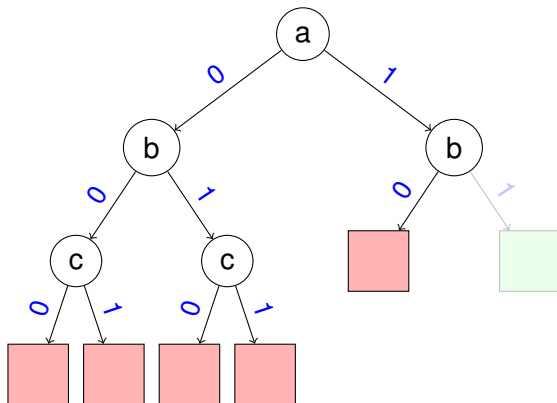
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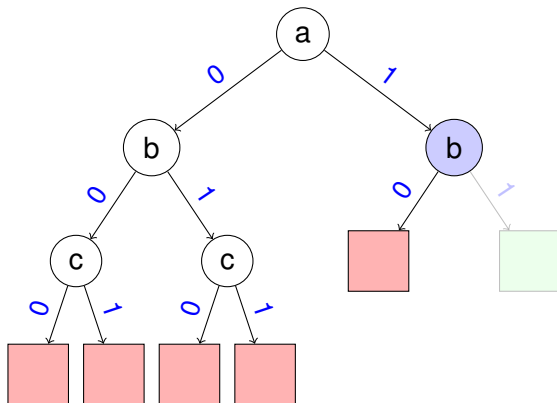
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$(a \vee \neg c \vee \neg d)$
$(\neg b \vee \neg c \vee d)$
$(\neg a \vee b \vee \neg c)$
$(\neg a \vee \neg b \vee c)$



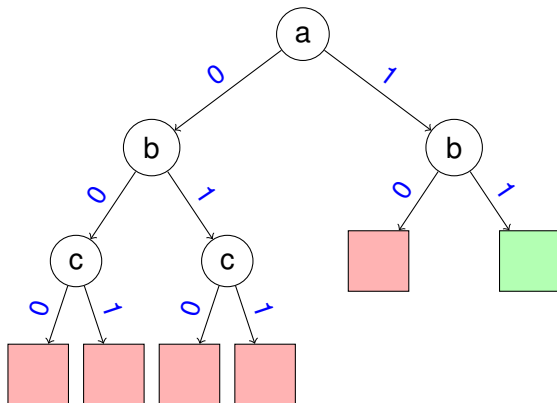
SAT Solving in a Nutshell

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 $(a \vee c \vee \neg d)$
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 $(\neg b \vee \neg c \vee d)$
 $(\neg a \vee b \vee \neg c)$
 $(\neg a \vee \neg b \vee c)$



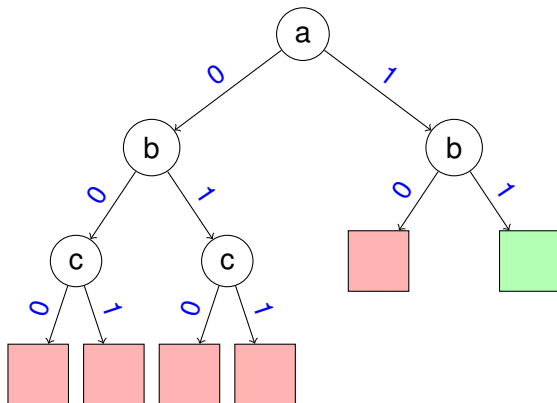
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 $(\neg a \vee \neg b \vee c)$



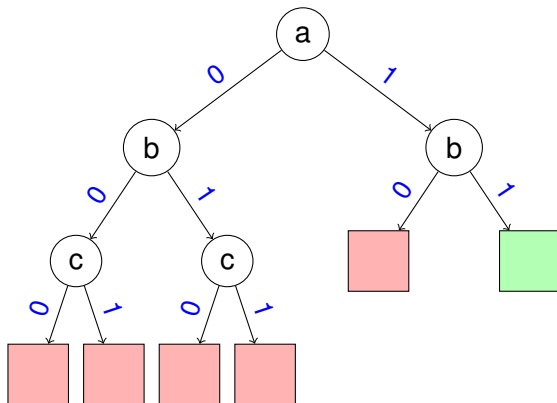
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 $(\neg b \vee \neg c \vee d)$
 $(\neg a \vee b \vee \neg c)$
 $(\neg a \vee \neg b \vee c)$



SAT Solving in a Nutshell

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 $(a \vee c \vee d)$
 $(a \vee c \vee \neg d)$
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 $(\neg b \vee \neg c \vee d)$
 $(\neg a \vee b \vee \neg c)$
 $(\neg a \vee \neg b \vee c)$



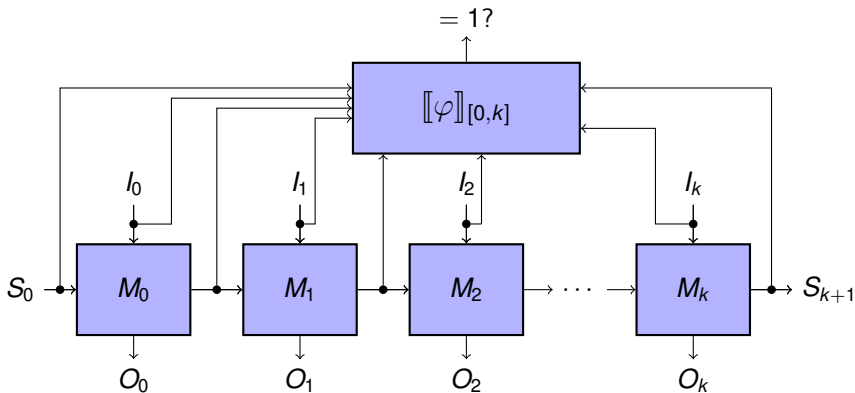
Advancements in SAT Solving

- **1962:** DPLL backtracking algorithm [Davis et al., 1962]
- **1996:** Conflict learning [Silva and Sakallah, 1996]
- **2001:** Local search, decision heuristics, engineering ...
- Modern solvers handle **millions** of variables and clauses
- Popular solvers:
 - MiniSAT
 - Glucose
 - Lingeling
- Extensions of SAT:
 - Satisfiability Modulo Theories (SMT)
 - Quantified Boolean Formulae (QBF)
 - Max-SAT

Summary Equivalence Checking and SAT

- Verifying correctness of hardware synthesis
- Separation of **verification problem** and **decision engine**
- Many more applications in hardware & software verification
- Convenient and **standardized APIs** for ease of use
- Active field of research

Bounded Model Checking



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