
Institut
Mines-Télécom

# On-Chip Interconnect Protocols

Tarik Graba, Sumanta Chaudhuri
<tarik.graba@telecom-paristech.fr>

# Plan

# An Example SoC : TI OMAP 5432

An Example SoC from TI.

OMAP Used in various mobiles/tablets. e.g Amazon Kindle (OMAP 4430).

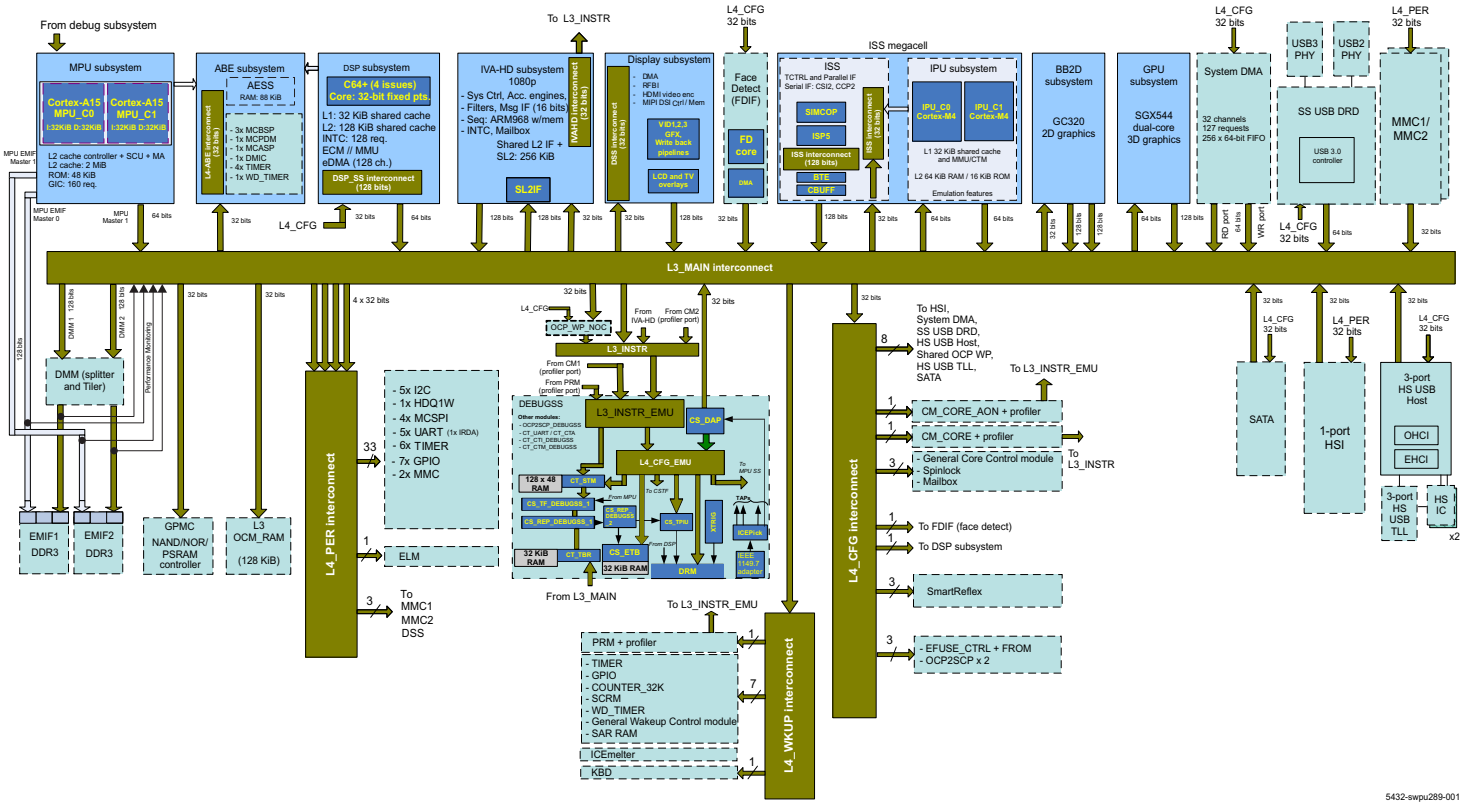


**Figure 1-1. OMAP5432 Block Diagram**

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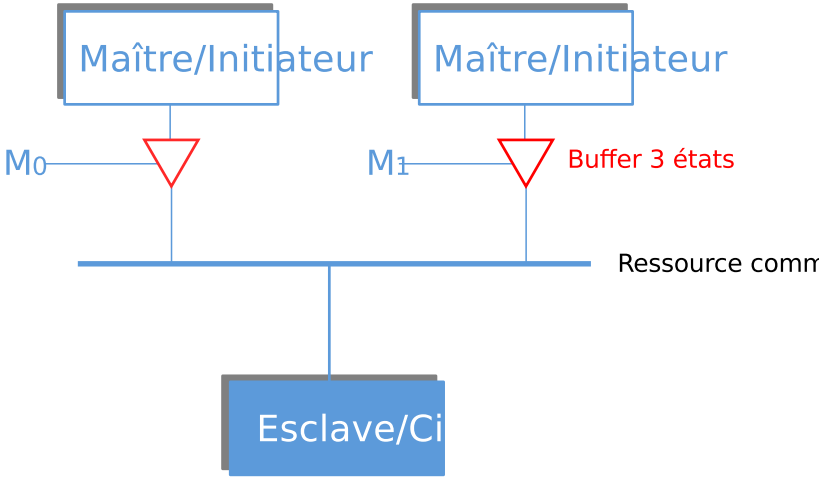
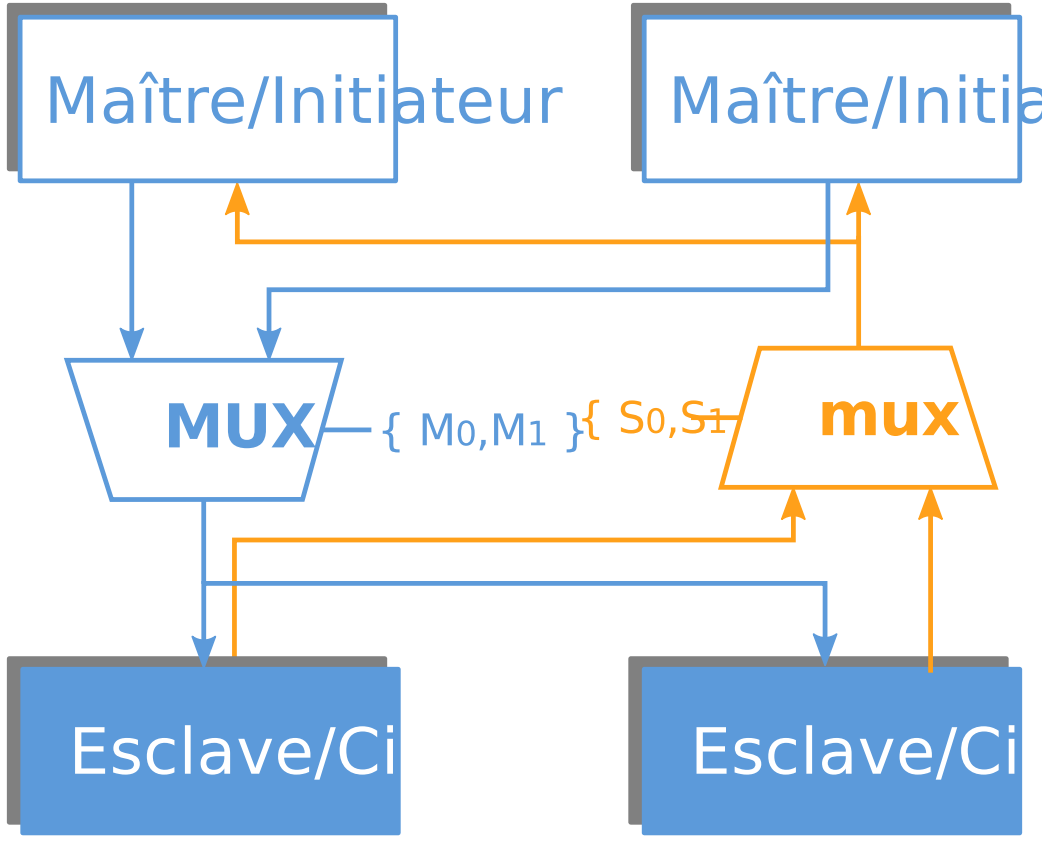
  - How do they communicate ?
  - Needs On-Chip Interconnect Protocols.

# History : Shared Bus




- All masters are connected to the same set of wires.
- A bus controller will issue token to masters to utilize the bus.
- One master blocks the bus.
- Huge capacitative loading..
- Not suitable for high performance applications.

# Modern Interconnect : Circuit Switched Network



# Modern Interconnect : Circuit Switched Network

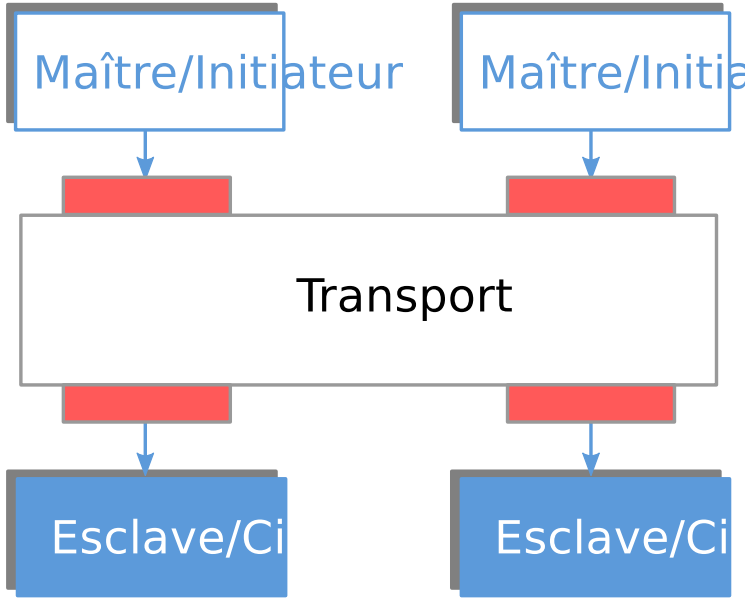
## Stratégie d'arbitrage

The arbiter switches from one master to another using a pre-defined strategy.

- Round Robin.
- Priority Base.
- Time-out Based.

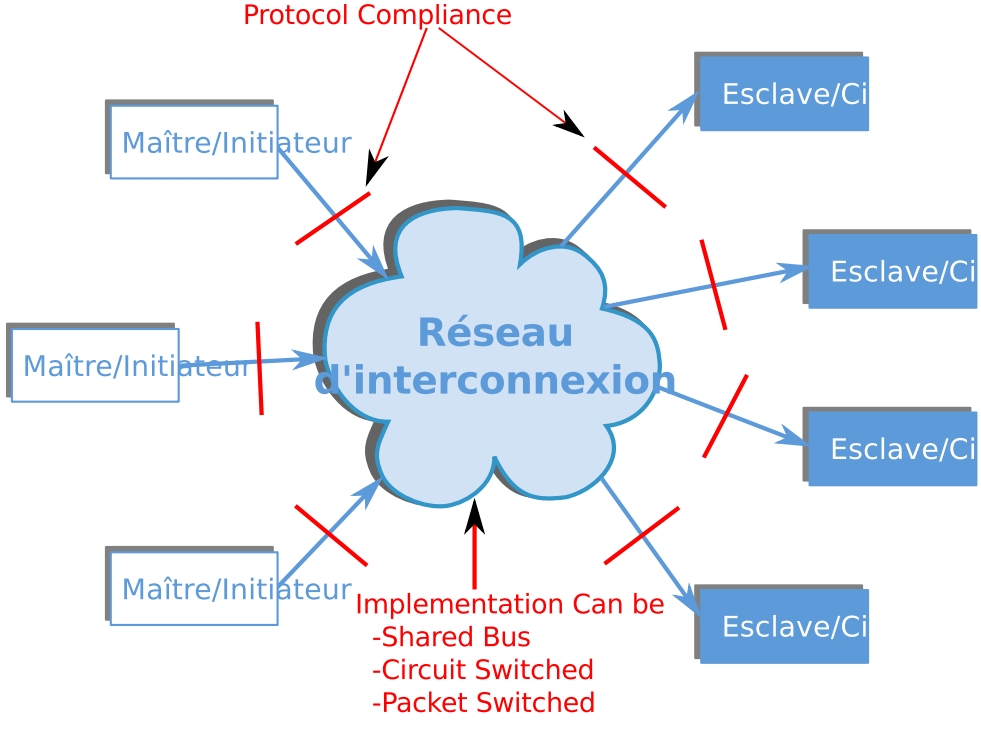
# Modern Interconnect : Packet Switched Network

- Transactions are transformed into network packets.
- Packets will follow an available route to the slave.
- Packet sizes and network topology are determined from application requirements.



# On-Chip Protocols : Point to Point

- Dissociates network implementation from IP interface.
- Helps in plug'n play.
- Only the interface needs to be protocol compliant.



# Design Goals for Modern Protocols

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- Point-to-Point Protocols. ( As opposed to shared bus)
- Pipelined/Non-Blocking. Can have multiple outstanding requests.
- Be suitable for DRAM Traffic. (Out-of-order data, initial access latency)

# Some On-Chip Interconnect Protocols

- AMBA (Advanced Microcontroller Bus Architecture)

  Open standard maintained by ARM.
- OCP-IP (Open Core Protocol International Partnership)

  Open standard developed by an industry consortium (TI, NXP, etc. etc.)
- Other standards include CoreConnect, VCI (Virtual Component Interface), STBus etc. etc.

# Quiz

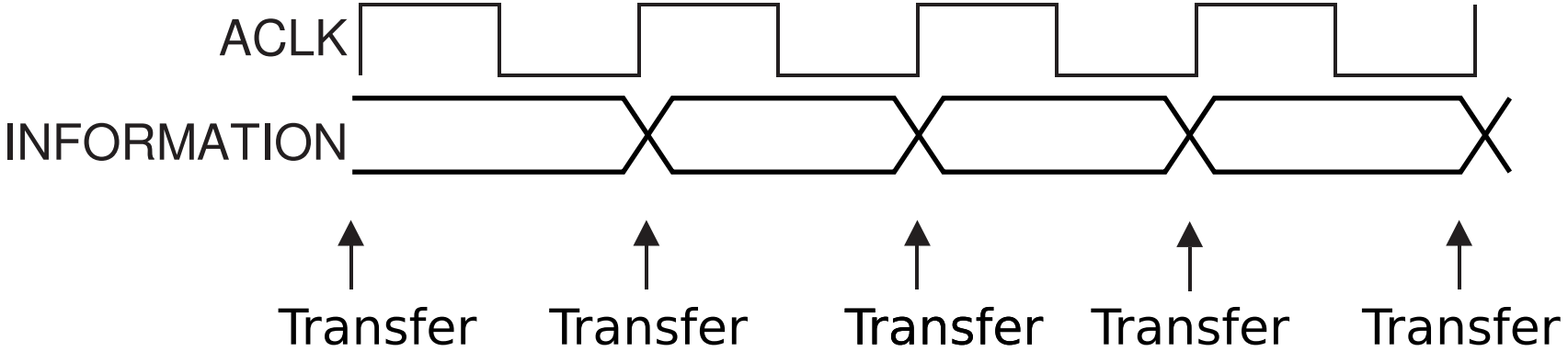
- What are the differences between On-Chip Networks & Off-chip Networks ?

# Plan

- We will discuss some basic concepts : Handshake, Memory-Maps etc.
- We will discuss the AXI3 Standard first.
- We will see the differences between AXI3 & AXI4.
- We will see the differences between AXI OCP.

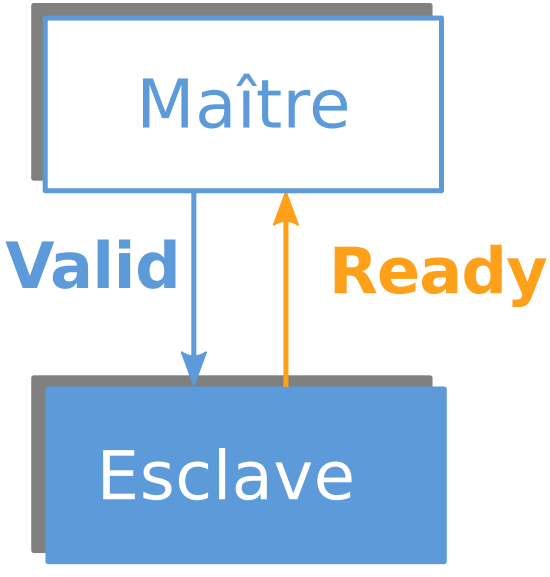
# Plan

# Basics : Clocked Interface



# Basics : VALID/READY Handshake

- A clocked interface can't be stalled.
- Handshake mechanism to include stalling behavior.



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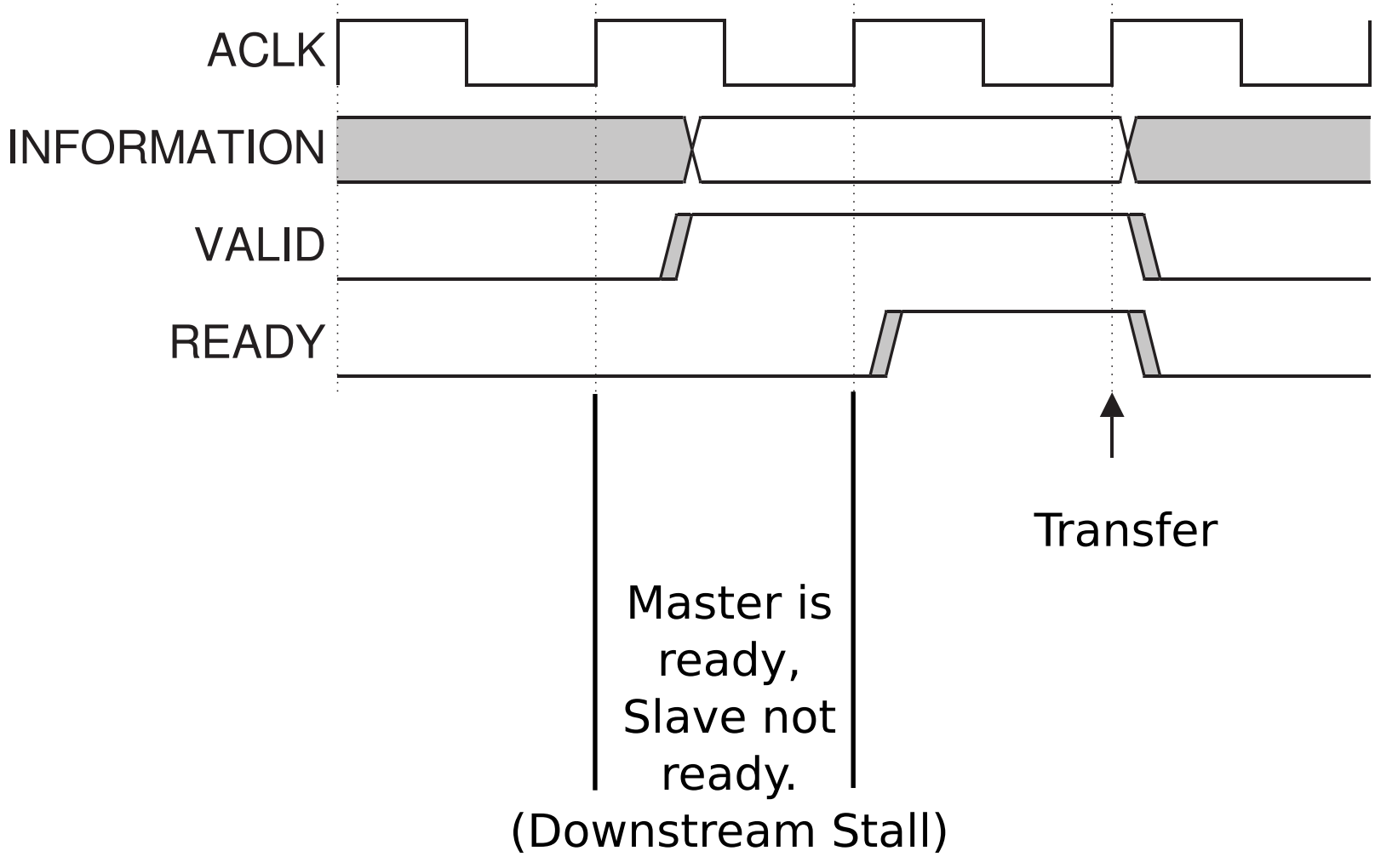

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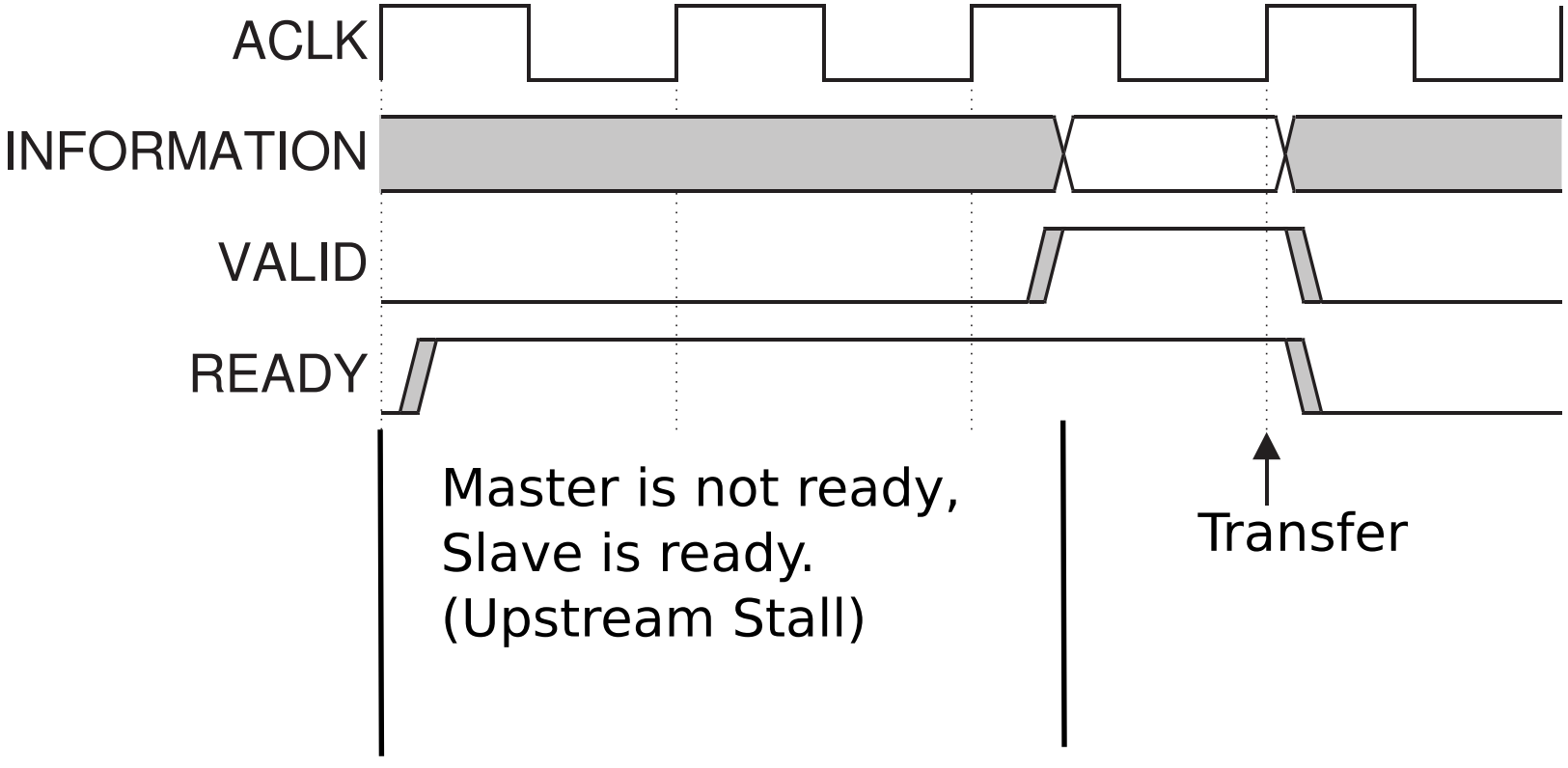


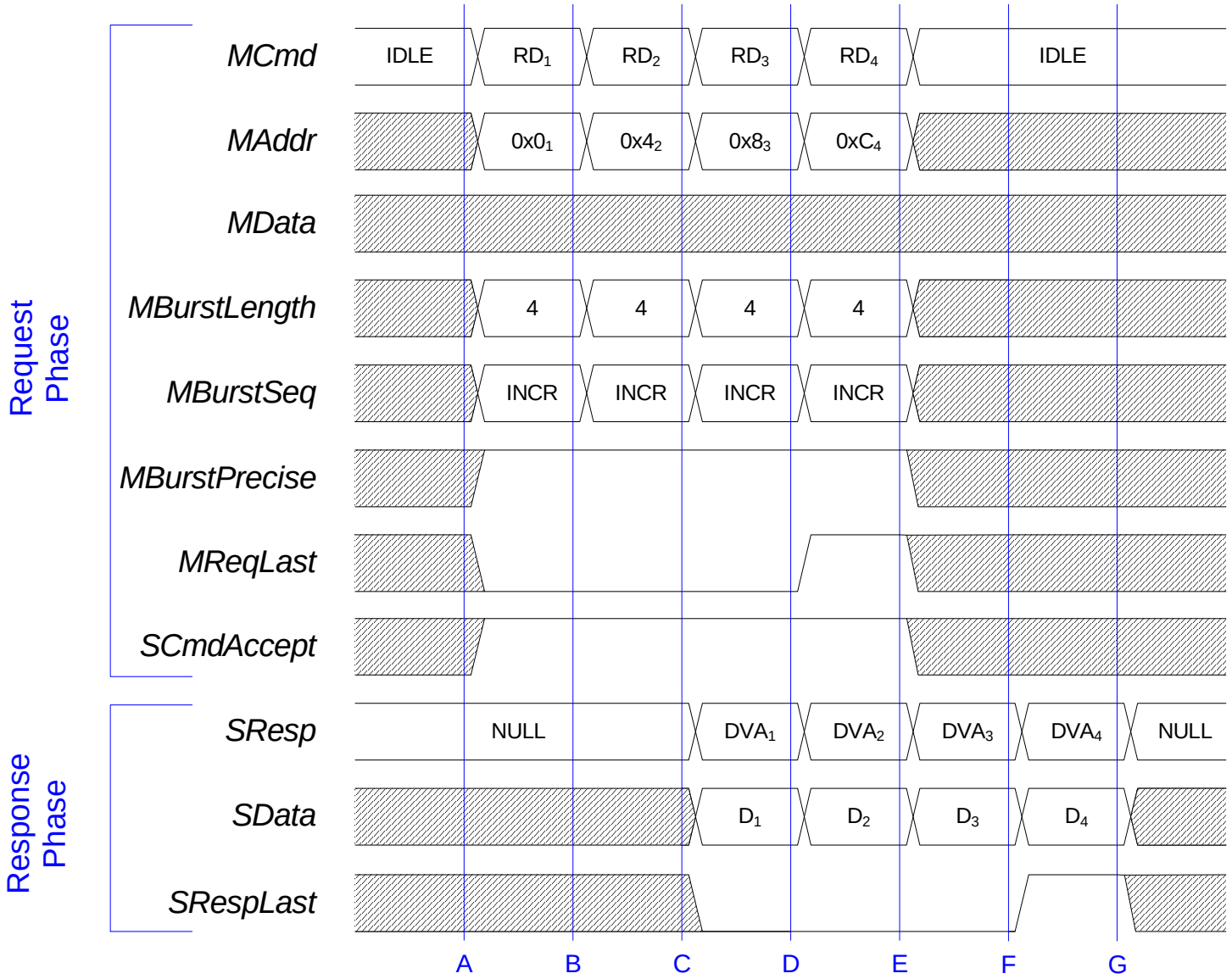
# Quiz

- What are the pros/cons for a valid/ready interface compared to clock interface ?
- When would use handshake and when would you use clocked interface ?

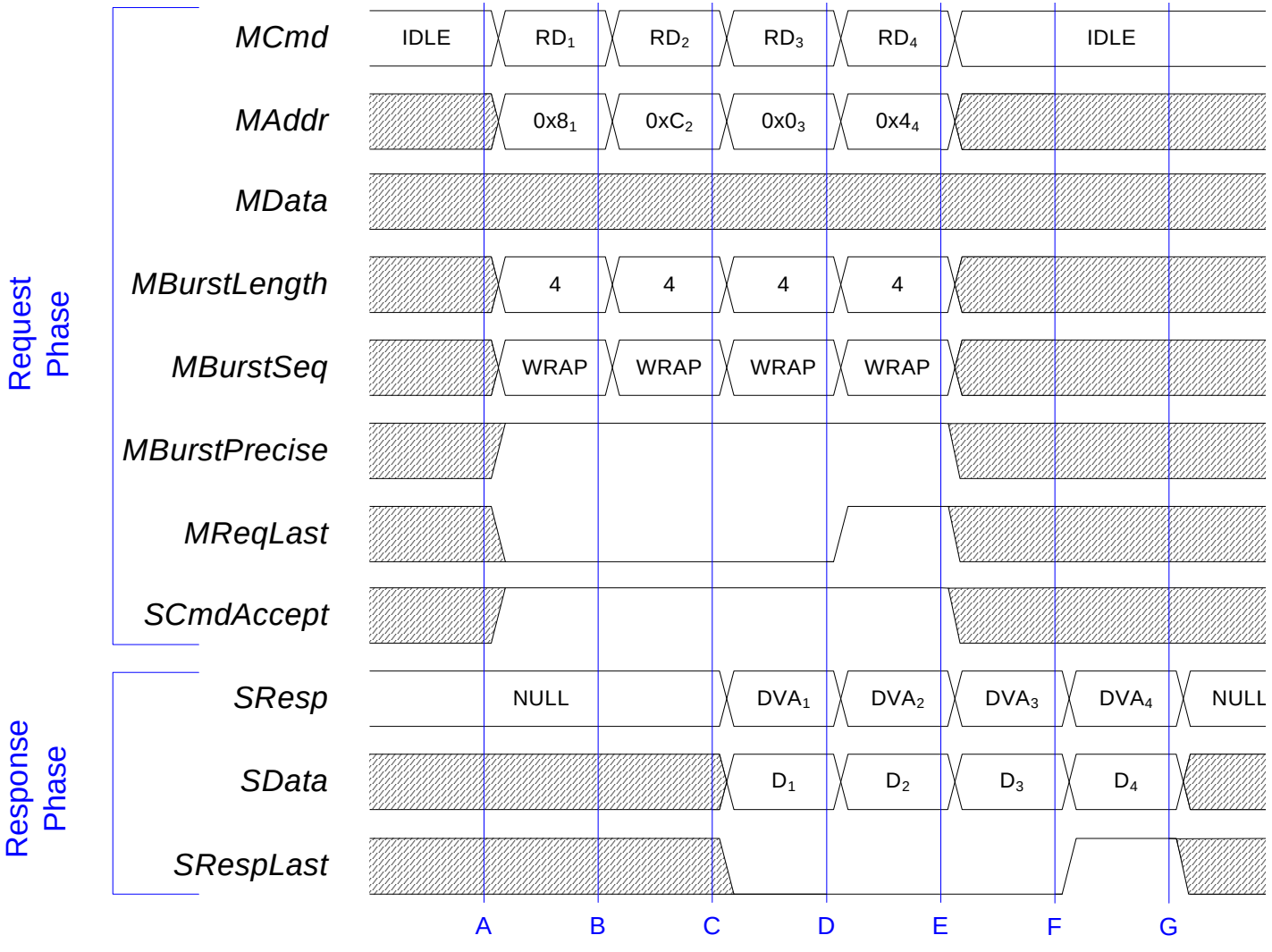
# Bursts

- Successive writes/reads to a predefined address pattern.
- e.g incremental (one dimensional), 2D Bursts.
- MRMD : Multiple Request Multiple Data.
- SRMD : Single Request Multiple Data.

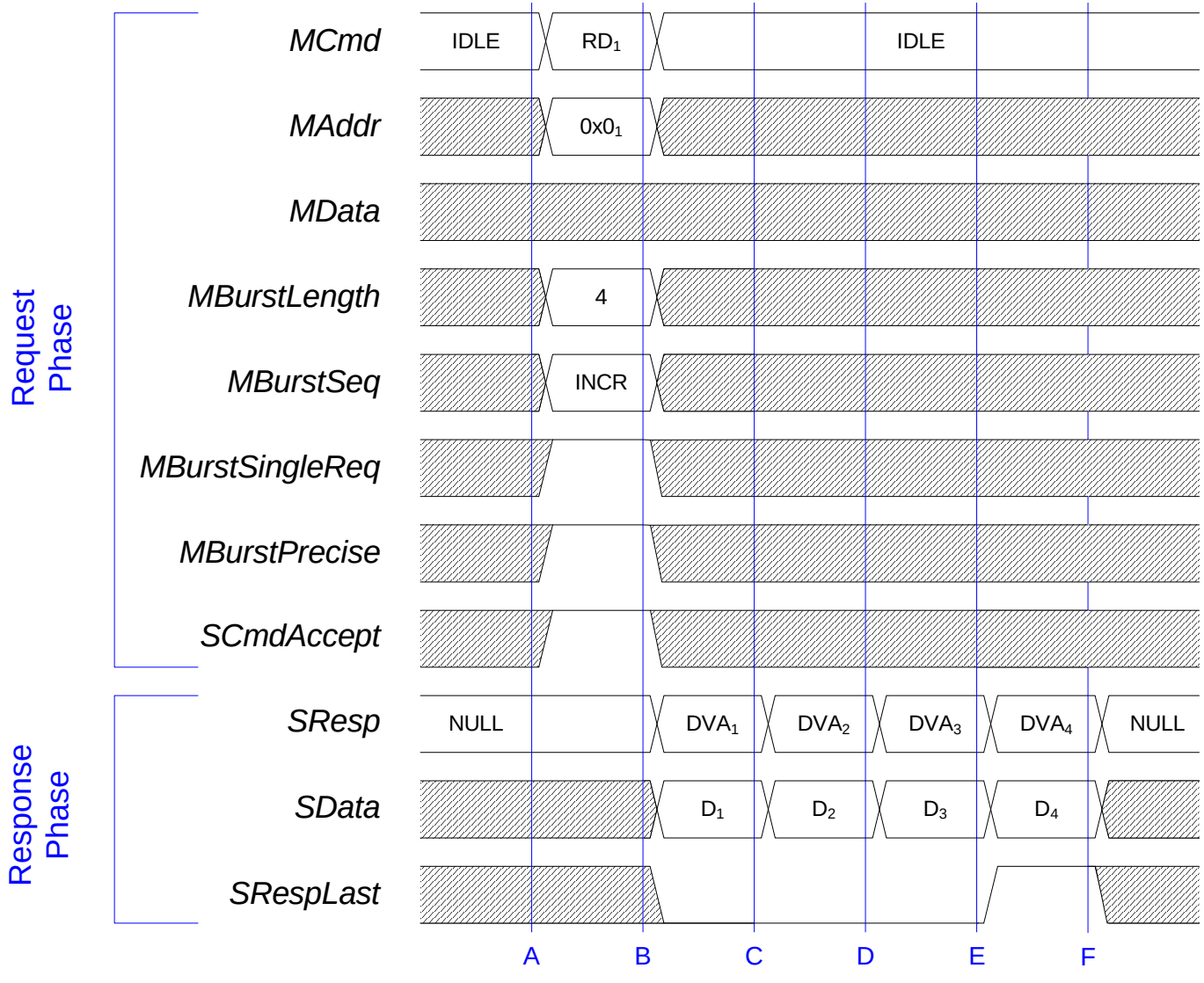
# Incremental Burst :MRMD



# Wrap Burst :MRMD



# SRMD Burst




C. The master captures the first response data. The slave issues the second

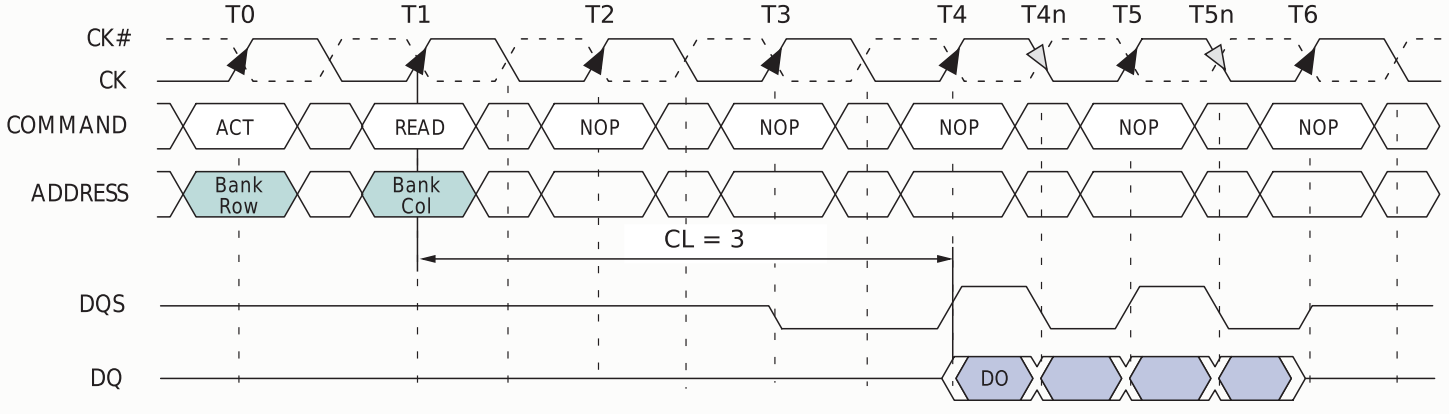
# Quiz

- A processor missed a data in the cache and wants to a cache-line fill. Which type of burst shall it use ?
- What is cache line size for common processors ARM/MIPS ?
- If the data width of the interface is 128 bits, how many cycles (minimum) are required for a cache line fill ?
- Which one is better ? SRMD or MRMD ?

# DRAM Traffic

## High Initial Latency

### Exemple d'une SDRAM



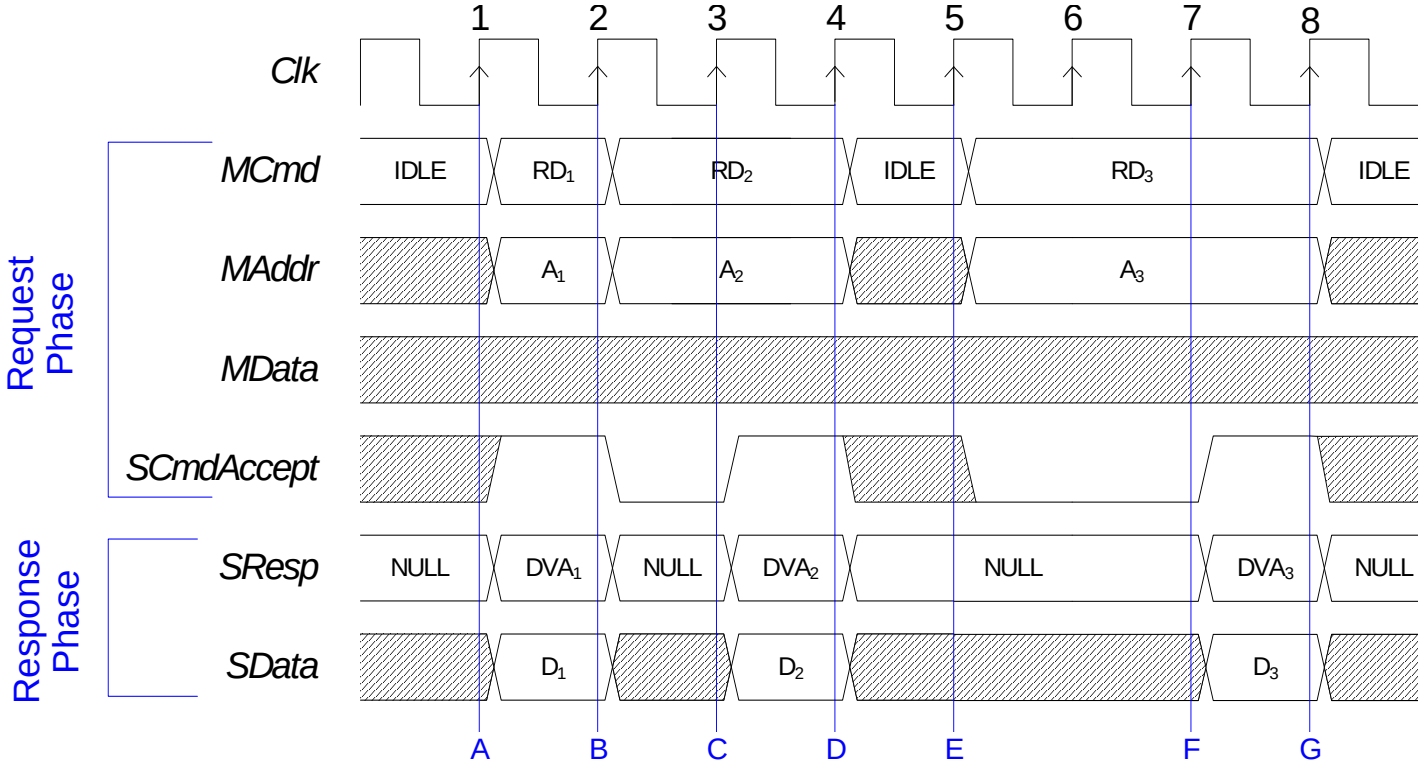

Source: Micron MT46V32M16 (DDR) SDRAM Datasheet

- DRAM is the main performance bottleneck in an embedded system.
- Protocols are designed for efficient utilization of DRAM.
- DRAM response can come out of order, has high initial latency

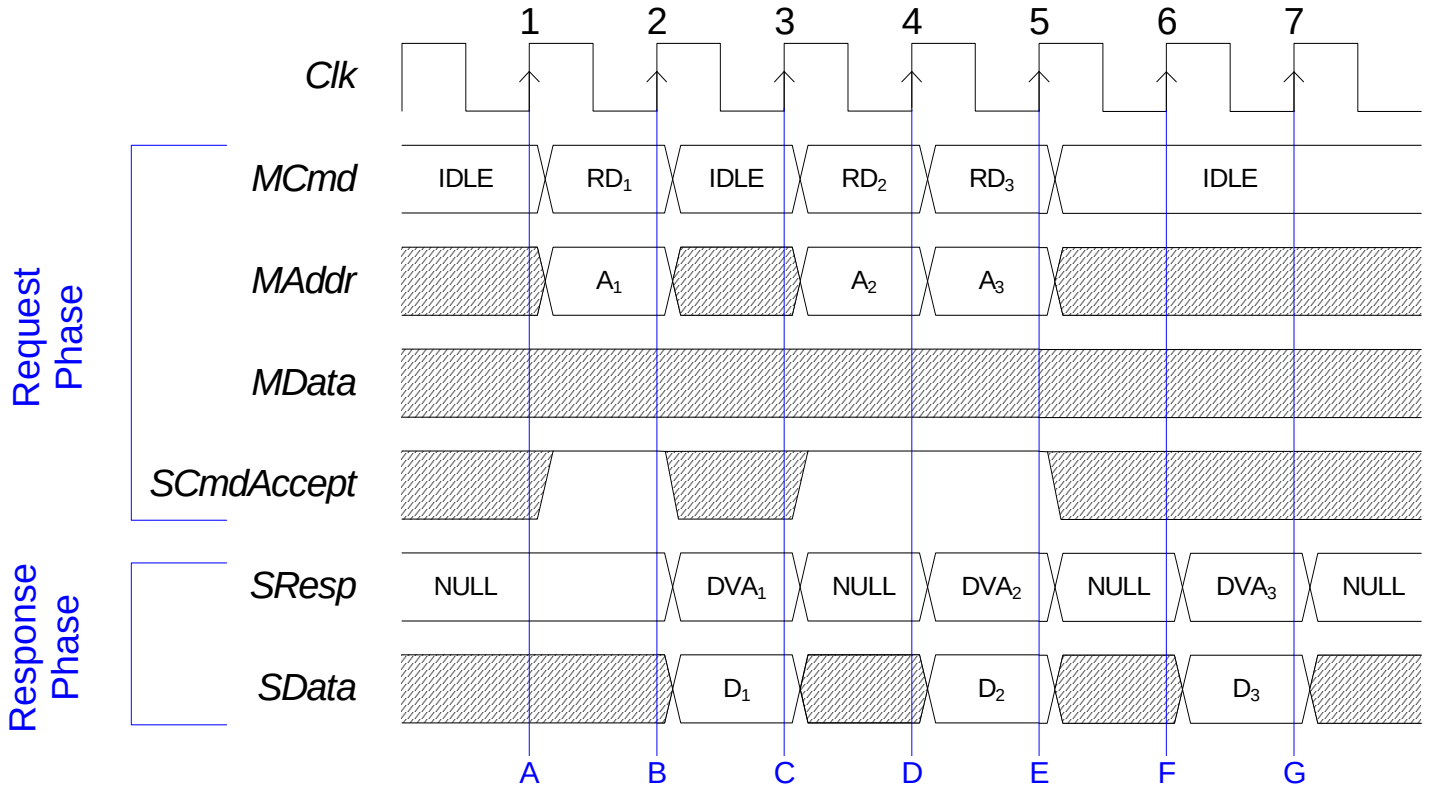
# Blocking & Non-Blocking

- Blocking :
  - Master doesn't emit a new request until the previous is finished.
  - Max. Outstanding Reads=1.
  - e.g AMBA (ARM Advanced Microcontroller Bus Architecture) (APB,AHB . . .), Wishbone
- Non-Blocking :
  - Master emits N requests before waiting for the responses.
  - Max. Outstanding Reads=N.
  - e.g AXI,OCP,VCI.

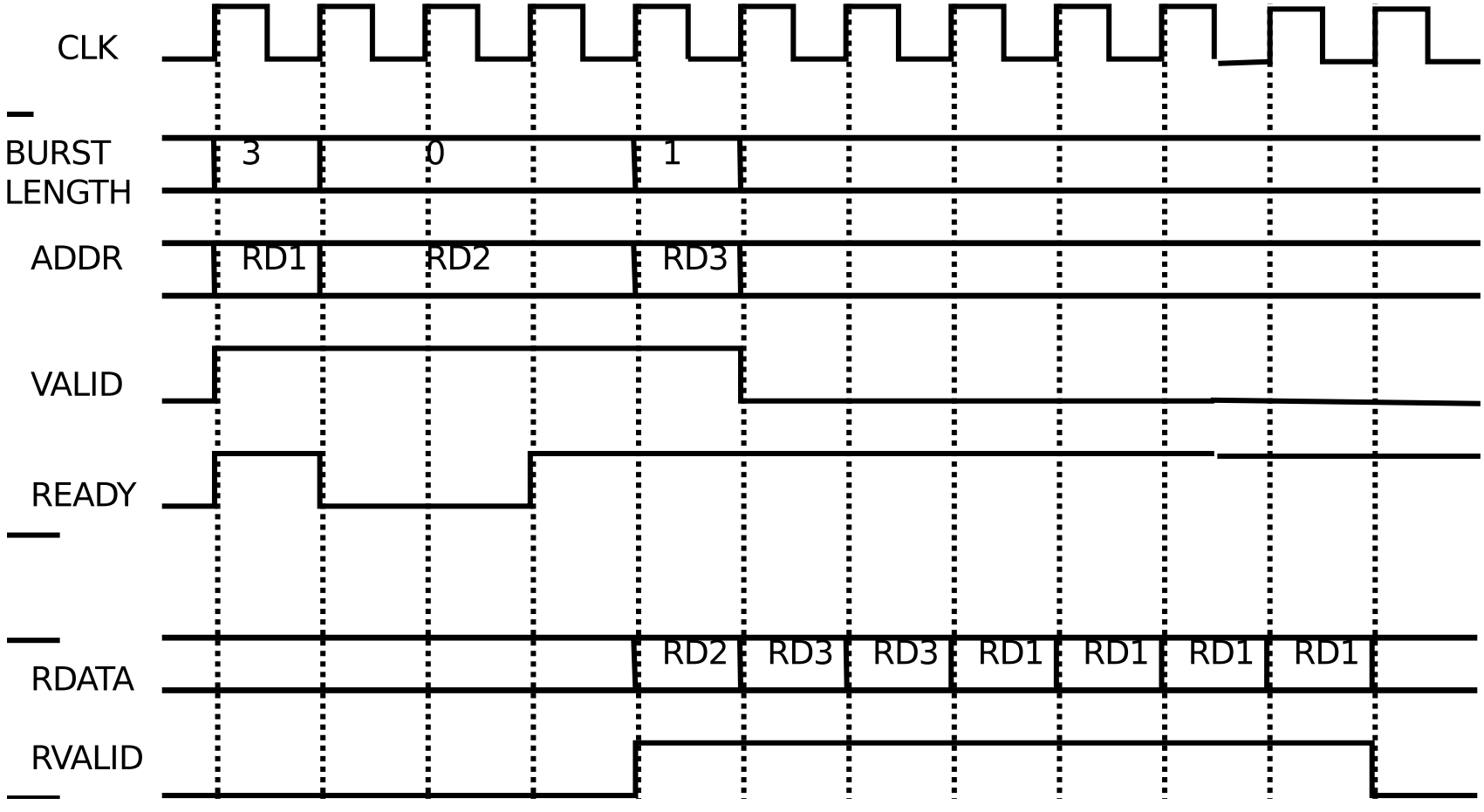
# Blocking Read



# Non-Blocking Read

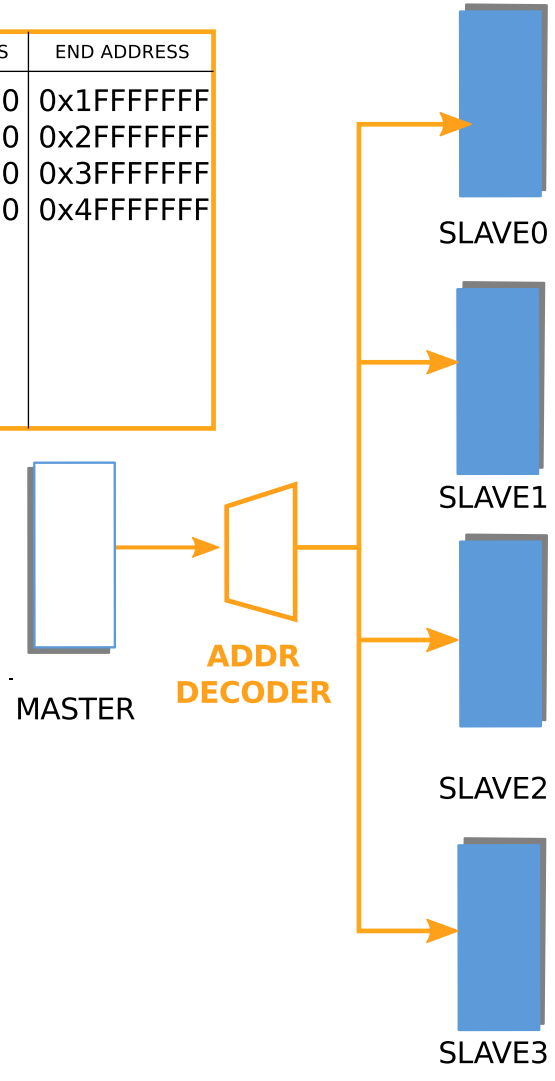


# Out-of-Order Execution

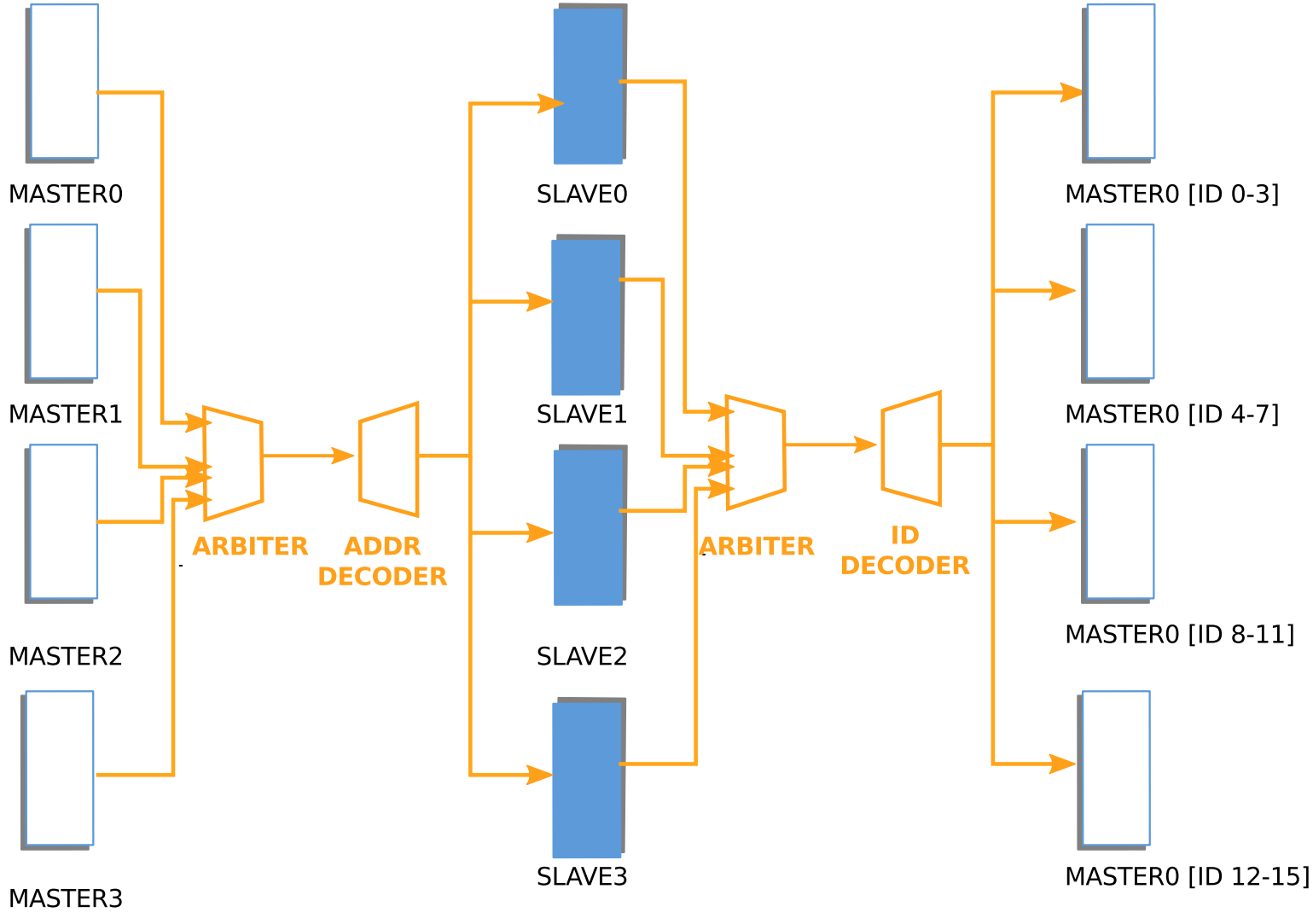


# Basics : Memory-Mapped Slaves

| TARGET | START ADDRESS | END ADDRESS |
|---|---|---|
| SLAVE0 | 0x00000000 | 0x1FFFFFFF |
| SLAVE1 | 0x20000000 | 0x2FFFFFFF |
| SLAVE2 | 0x30000000 | 0x3FFFFFFF |
| SLAVE3 | 0x40000000 | 0x4FFFFFFF |



# Basics : REQUEST & RESPONSE PATH



# Quiz

- An IP has a databus width of 128 bits. The average read latency from IP to DRAM is 32 cycles. In the return path the IP needs an average bandwidth of 16 bytes/cycle. How many outstanding read requests should it issue ?
- Is there a maximum limit on no. of outstanding reads ?

# Plan

# AMBA History

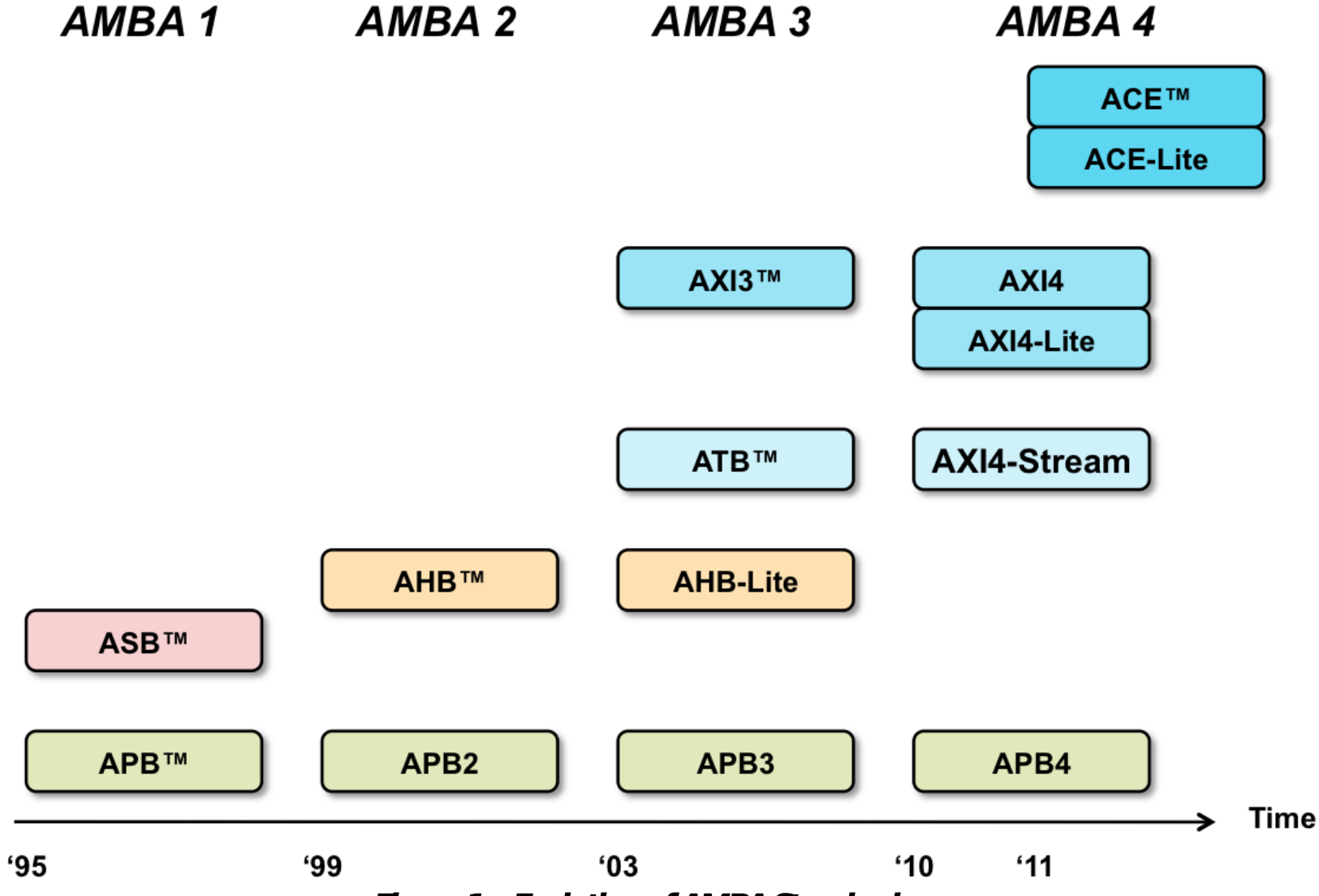
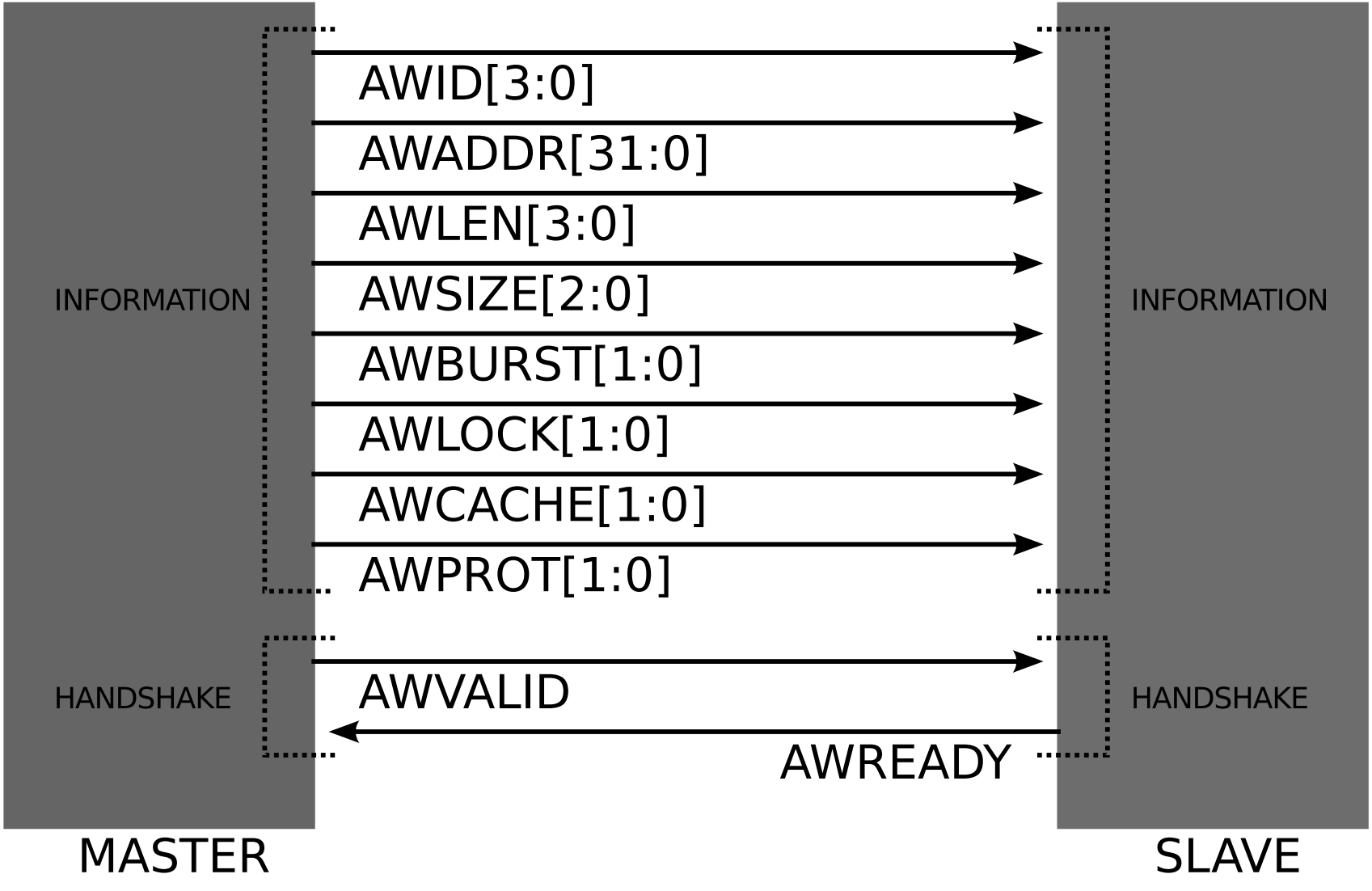



*Figure 1 – Evolution of AMBA Standards*

# AXI3 WRITE ADDRESS CHANNEL



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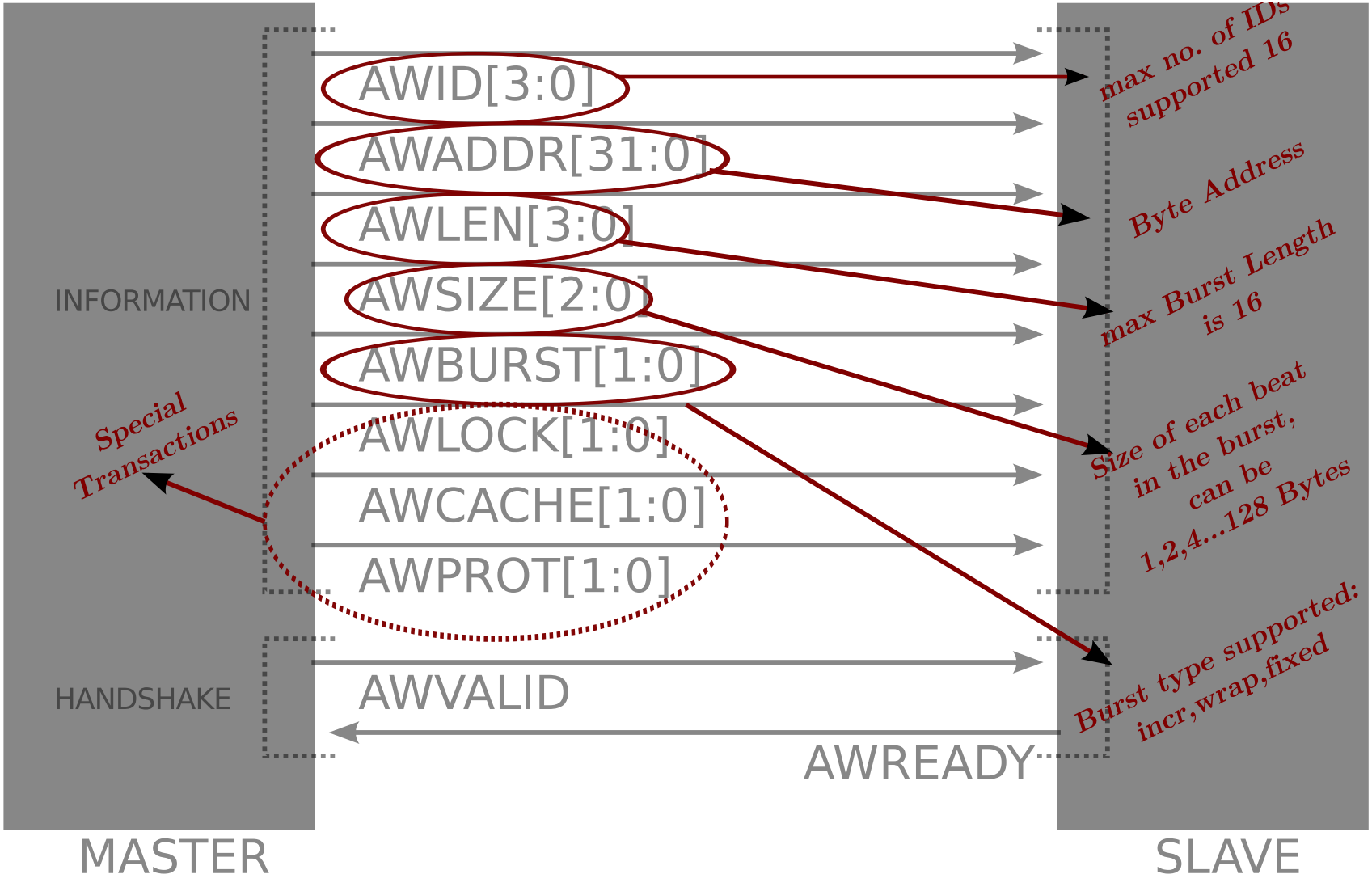
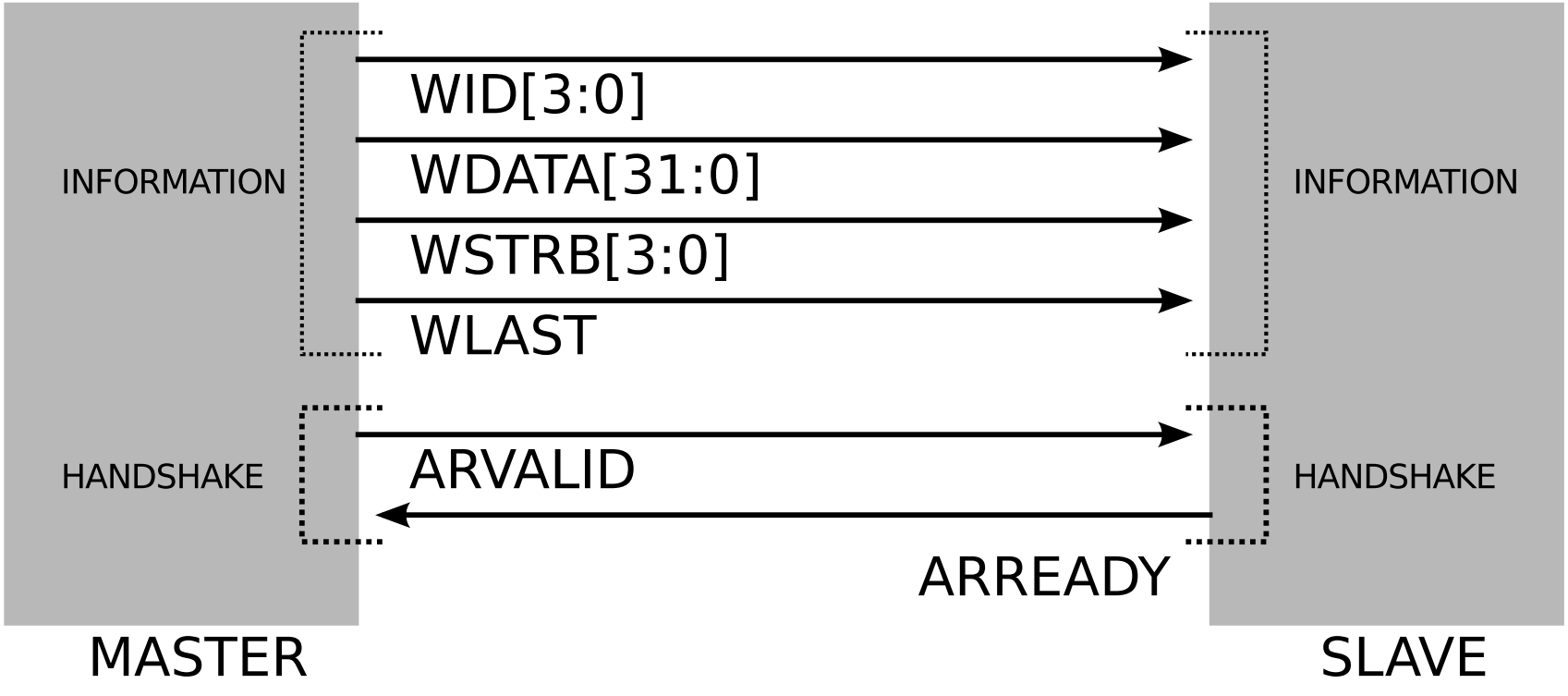


# AXI3 WRITE DATA CHANNEL



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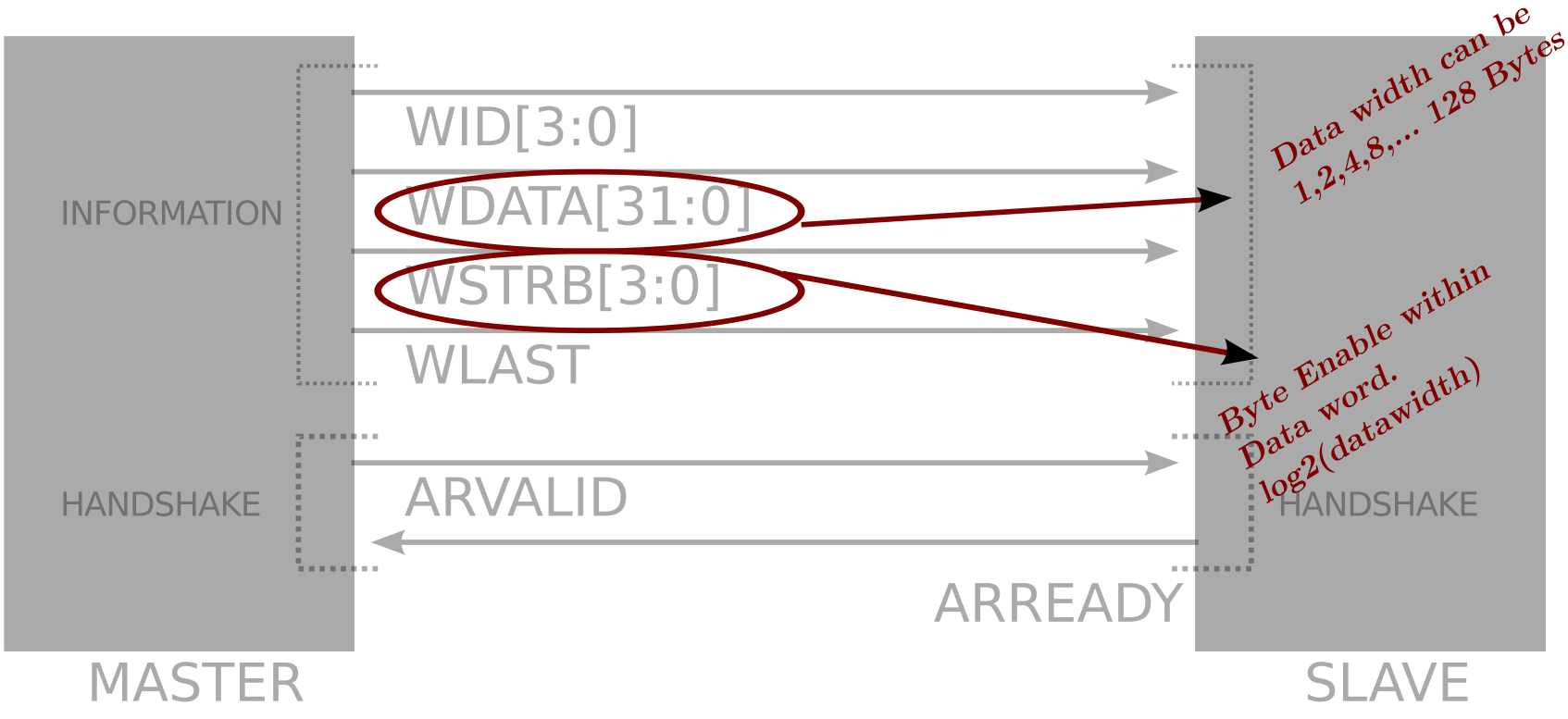
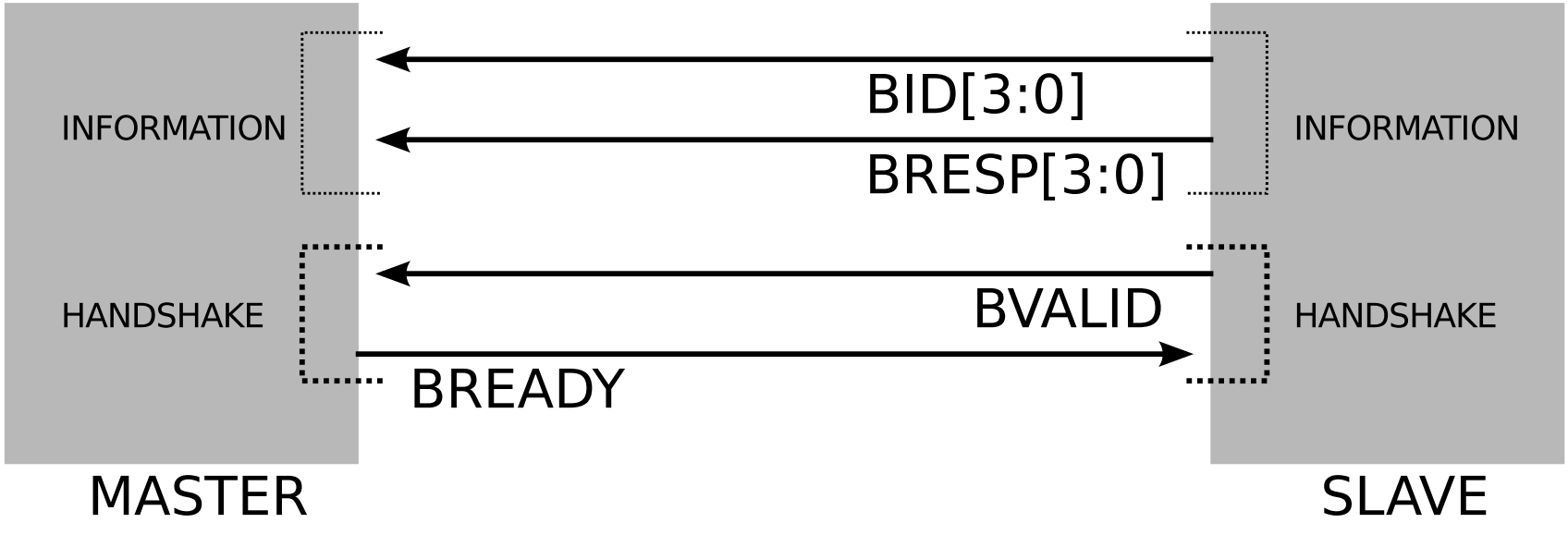


# AXI3 WRITE RESPONSE CHANNEL



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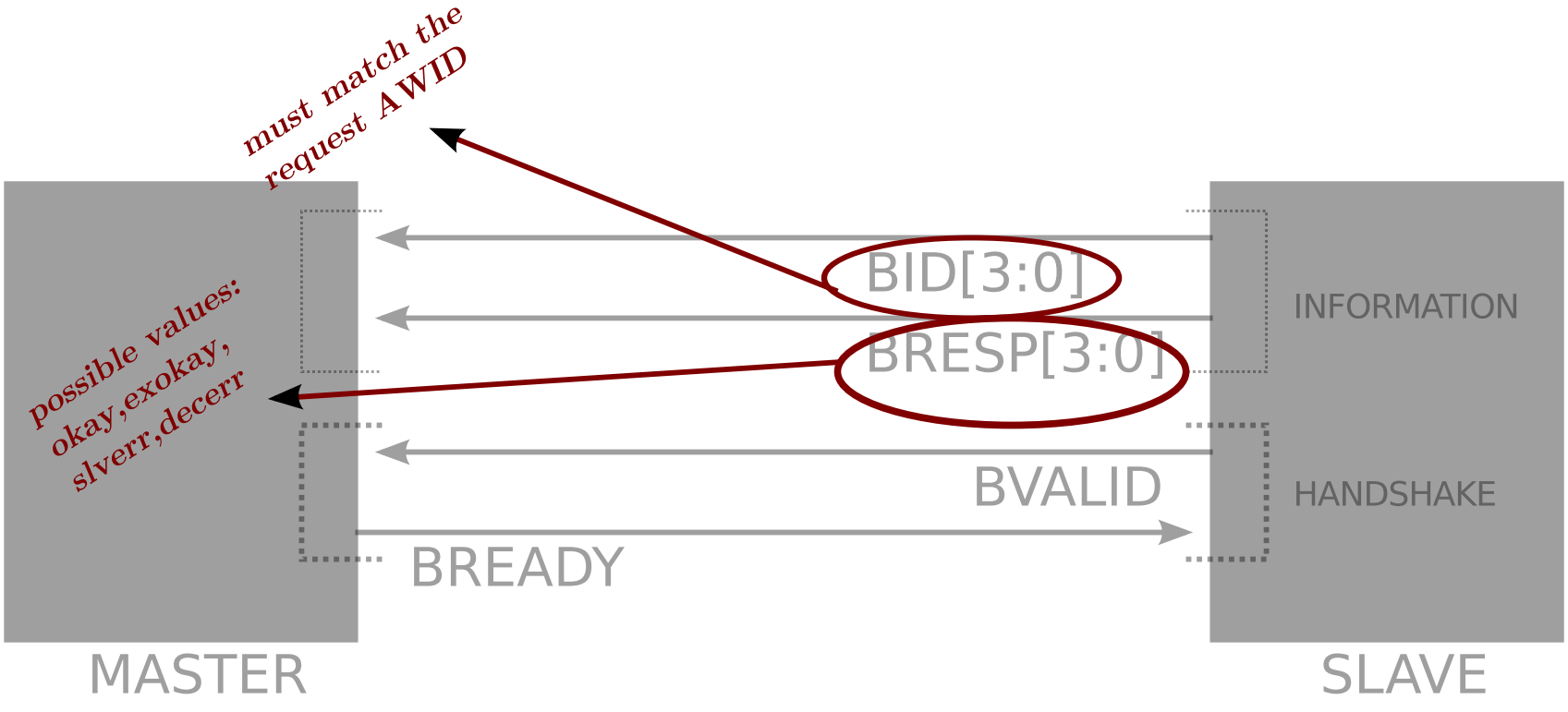
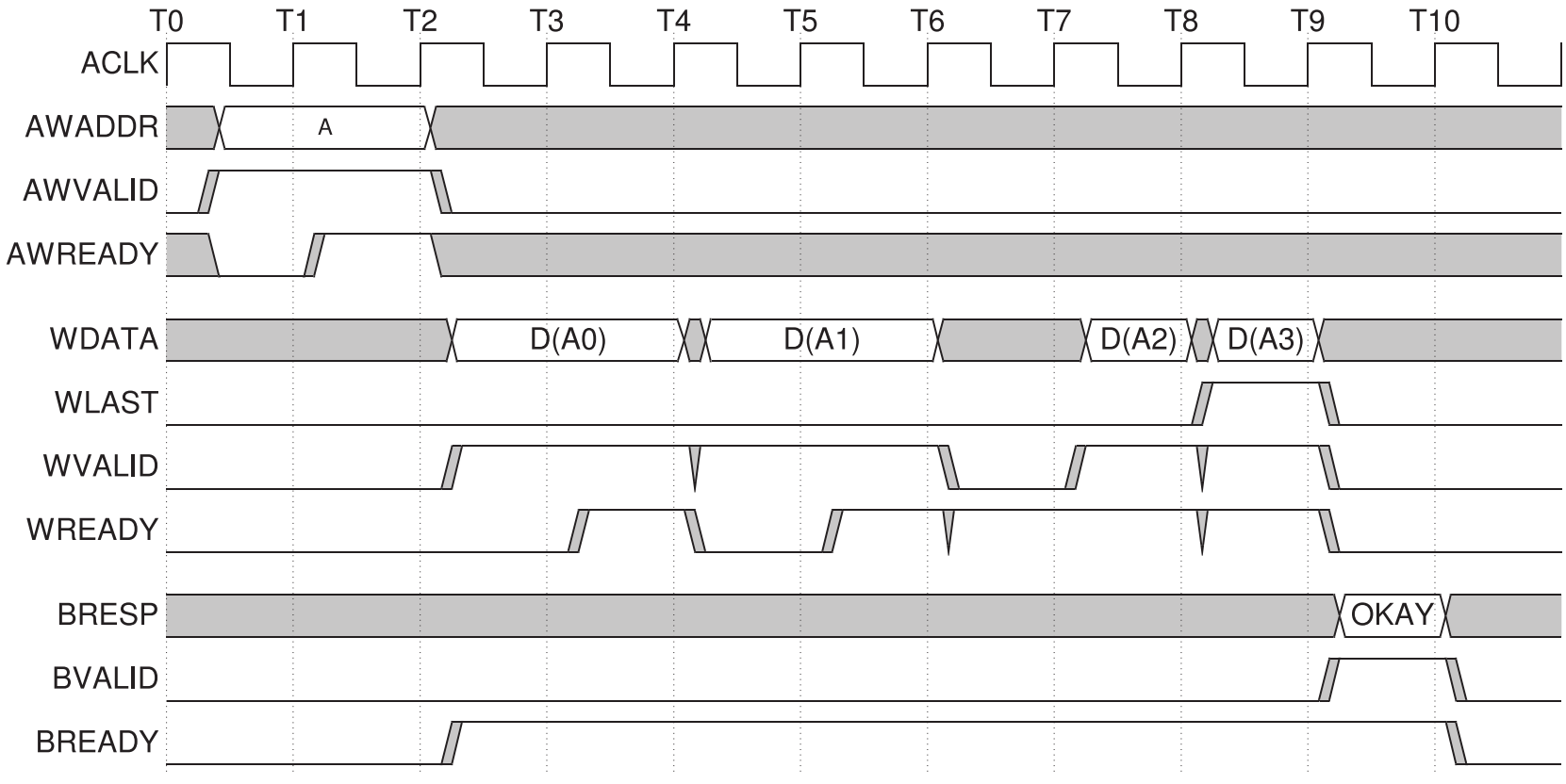
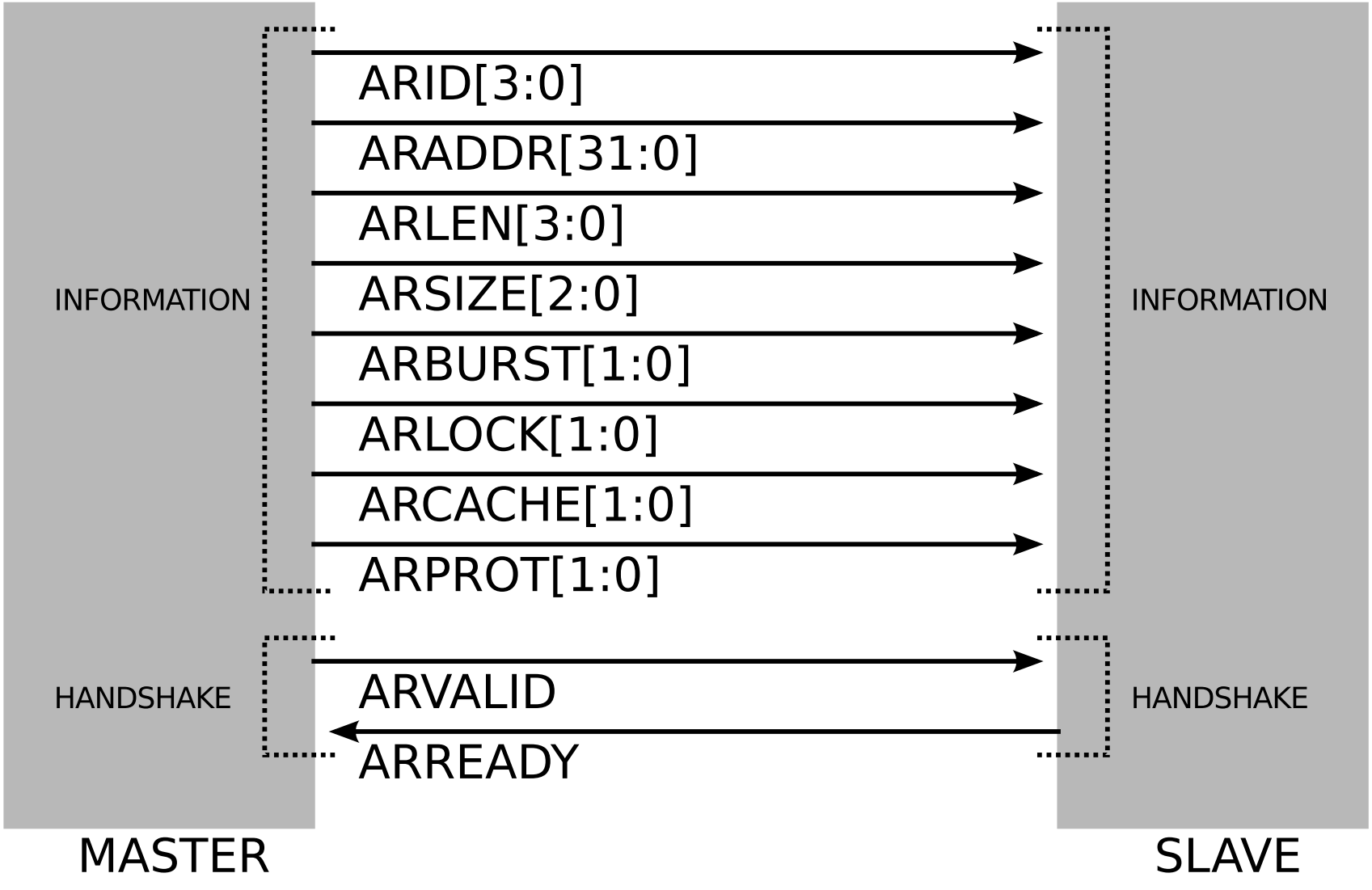


# AXI3 WRITE BURST



# AXI3 READ ADDRESS CHANNEL



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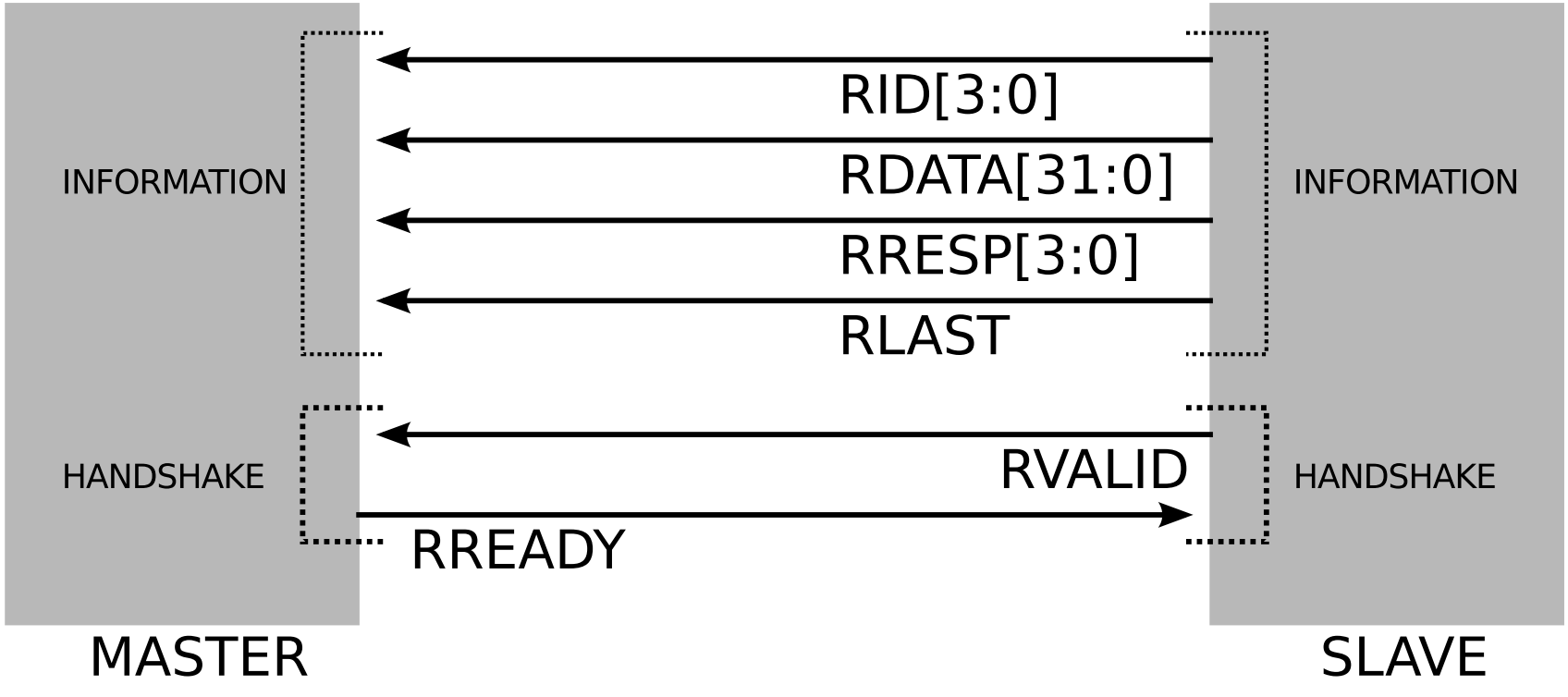

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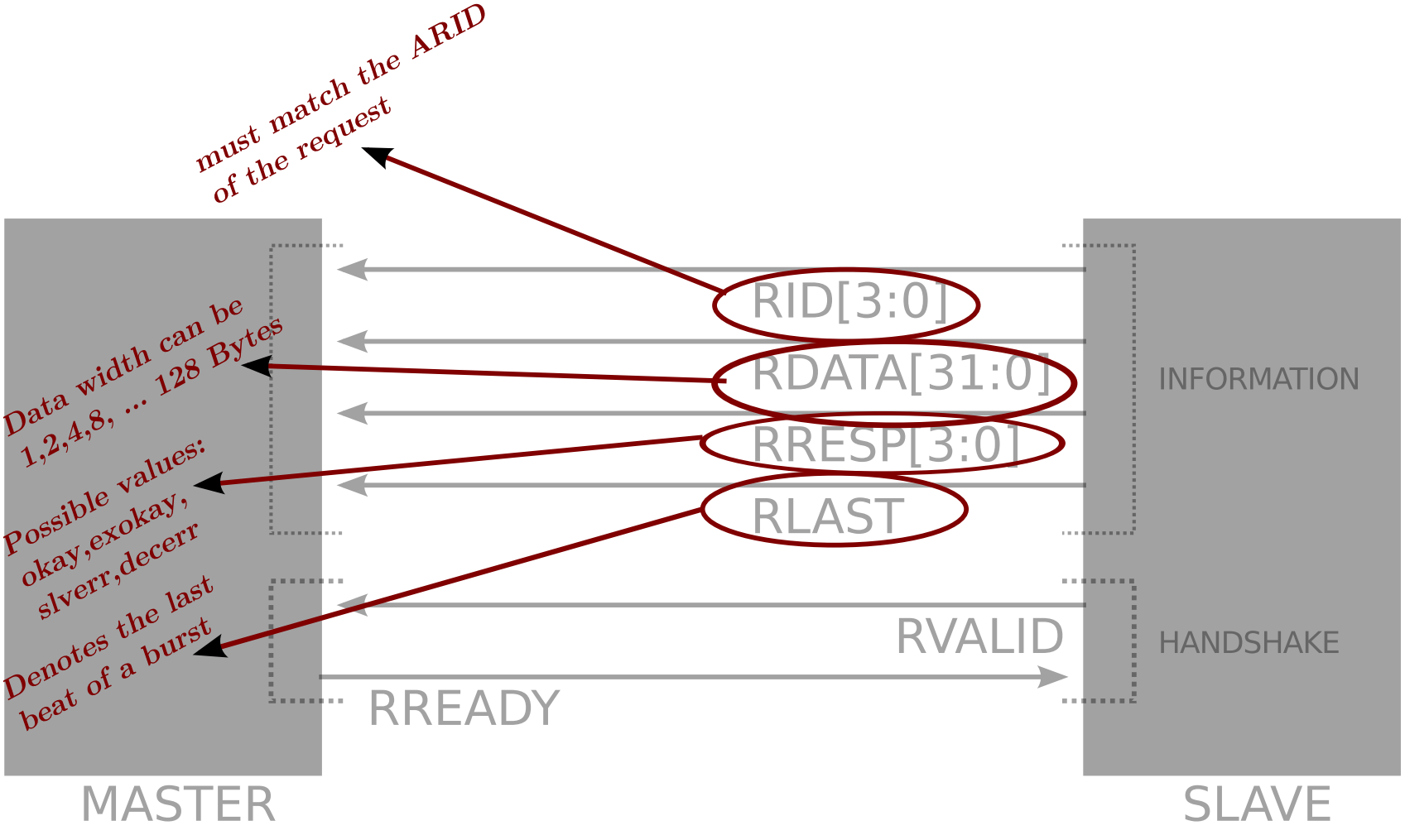

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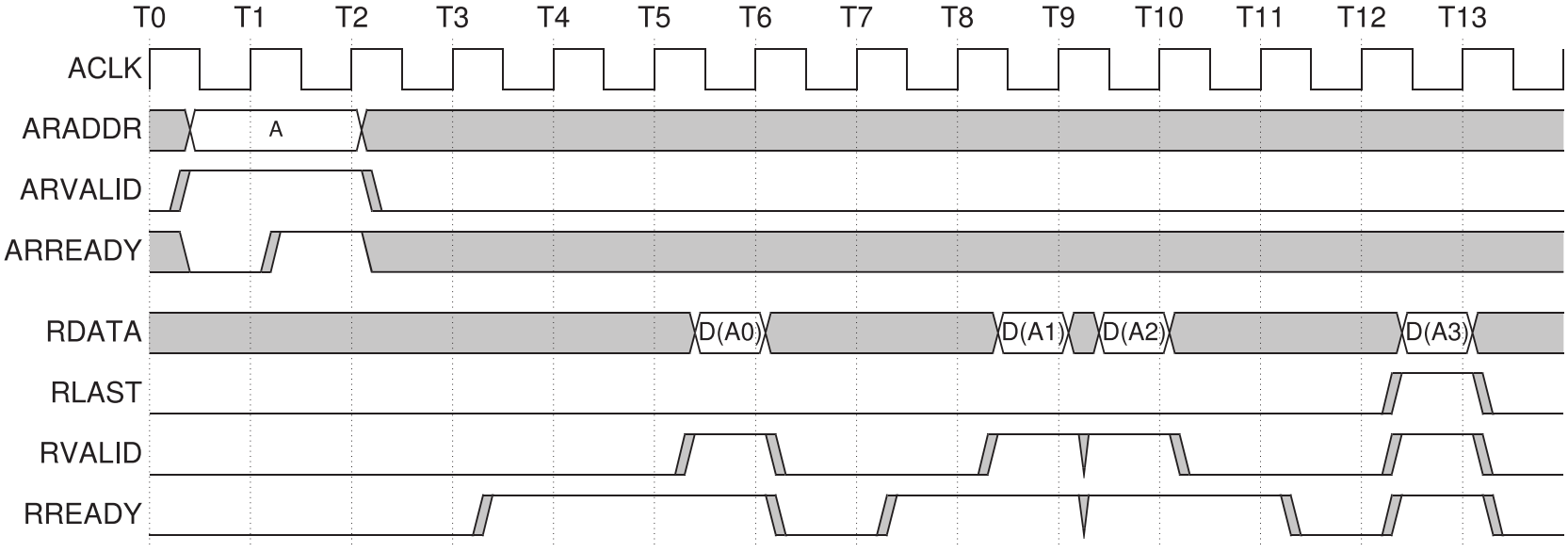

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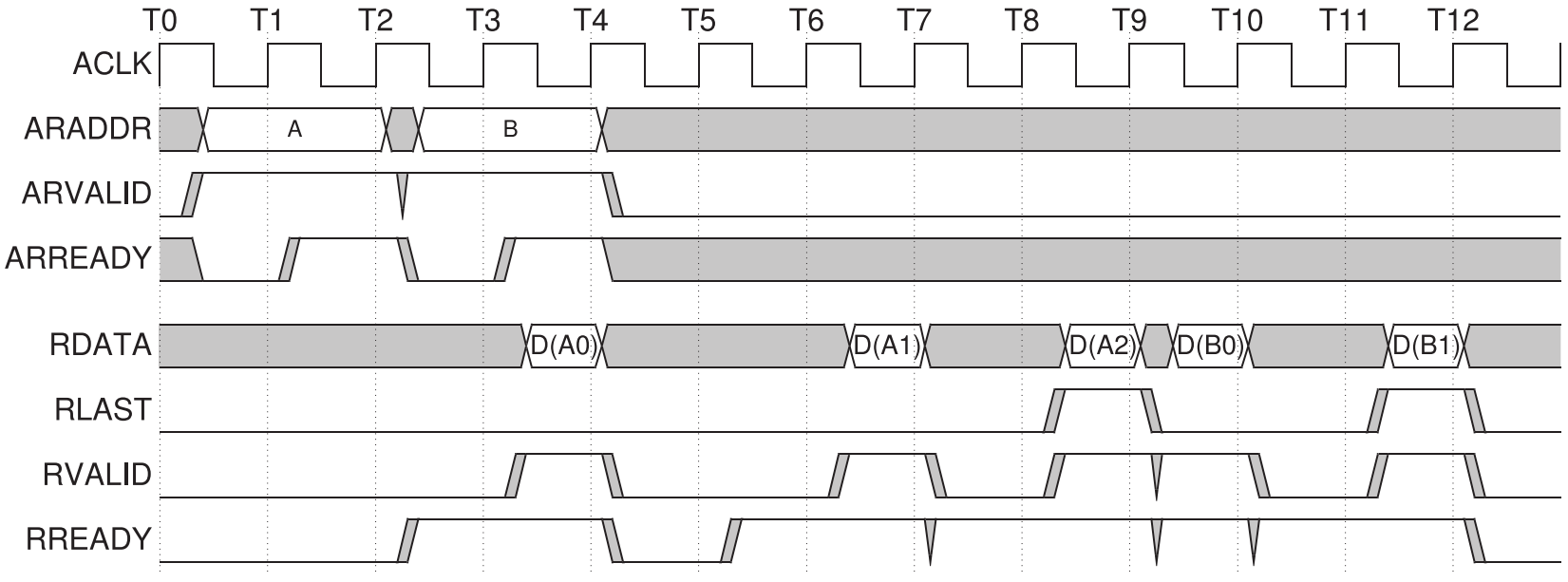
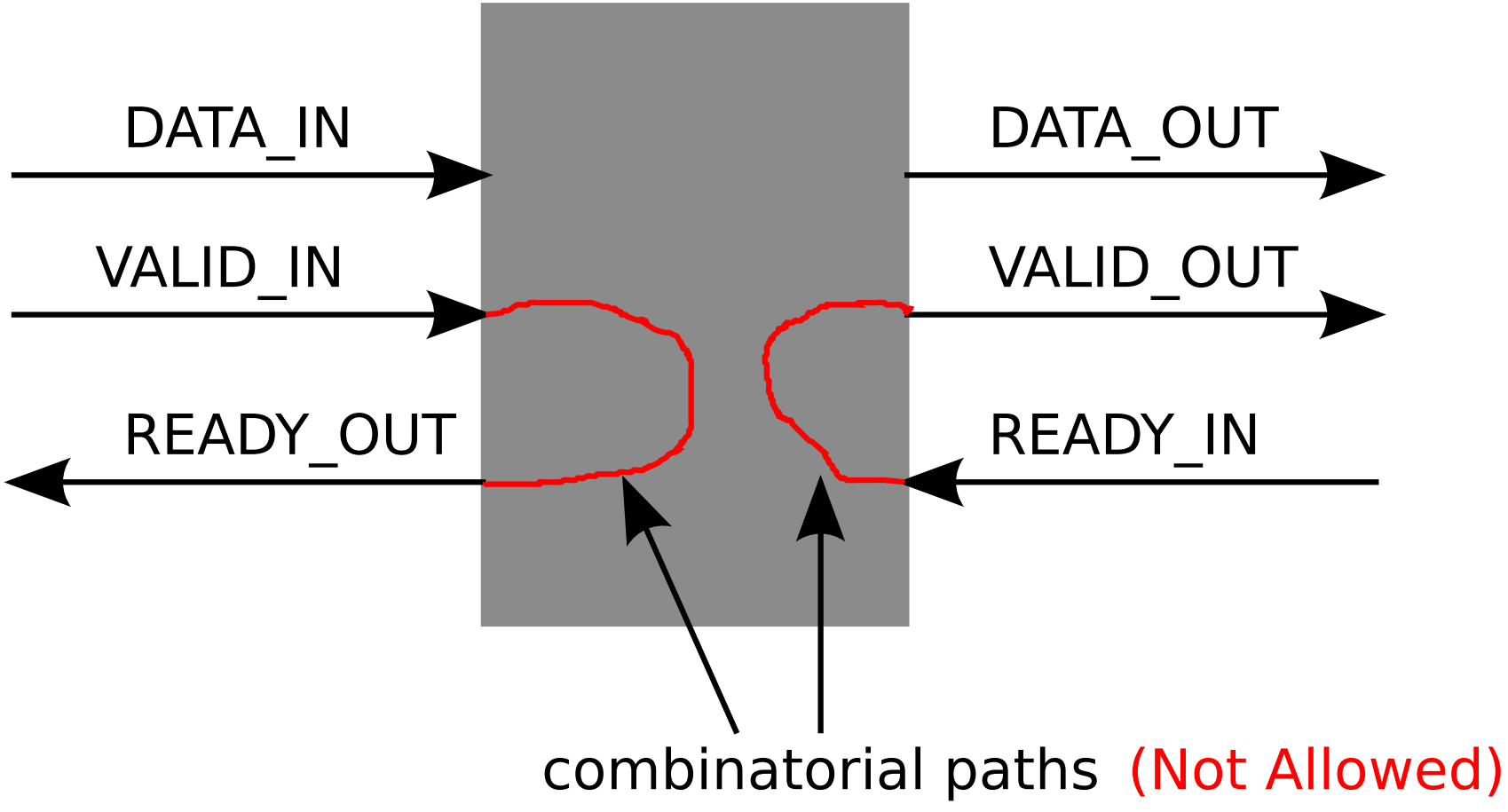


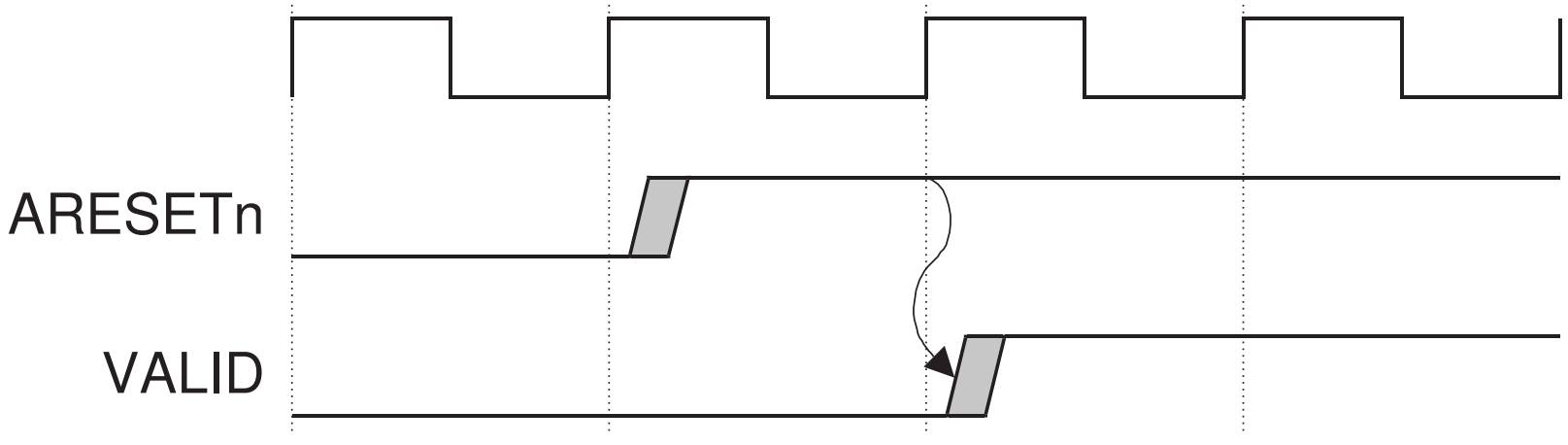
# AXI HIGHLIGHTS : Combinatorial Paths

- There must be no combinatorial paths between input and output signals on both master and slave interfaces.



# AXI HIGHLIGHTS : Reset

- The AXI protocol includes a single active LOW reset signal, ARESETn. The reset signal can be asserted asynchronously, but deassertion must be synchronous after the rising edge of ACLK.
- To avoid metastability associated with asynchronous de-assertion of Reset.



# AXI HIGHLIGHTS : Ordering Rules

- Key to Out-of-Order Transactions Processing.
- At a master interface, read data with the same ARID value must arrive in the same order in which the master issued the addresses.
- In a sequence of read transactions with different ARID values, the slave can return the read data in a different order than that in which the transactions arrived.

# AXI HIGHLIGHTS : Write Data Interleaving

- Write Data with different AWIDs can be interleaved.
- Not supported anymore in AXI4.

# AXI HIGHLIGHTS : 4K Crossing

- Bursts must not cross 4KB boundaries.
- This is enforced so that a burst doesn't cross over to another slave.
- The slave memory maps has to be aligned to 4KB boundaries.

# AXI HIGHLIGHTS : Special Transactions

- Cache Related Transactions. Used to indicate cache allocate and write policy.
- write policy
  - write-back : Processor writes data to cache. Cache writes the data back to main memory, when the system bus is free.
  - write-through : The processor write is complete only when the data has reached both main memory and cache..
- allocate policy :
  - Cacheable
  - Buferable.
  - Allocate/ Don’t allocate a cache line.
- Total 16 different cache related special transactions. (AxCACHE[3 :0]) x=RD/WR

# AXI HIGHLIGHTS : Special Transactions

- To indicate protected accesses. AxPROT[1 :0]
- Exclusive Access
  - implemented in the slave.
  - Signalled by AxLOCK[1 :0], BRESP[1 :0],RRESP[1 :0].
  - e.g an exclusive write is successful (denoted by EXOKAY) if no other master has written to the address space between previous read and the write to the same location.
- Locked Access
  - implemented in the the network.
  - Signalled by AxLOCK[1 :0].
  - The network guarantees that only the master is allowed access to a region, until an unlocked access comes from the same master.

# Features not supported in AXI4

- Locked transaction is no longer supported.
- WID signal disappears. Write Data interleaving is no longer supported.

# Additional Features in AXI4

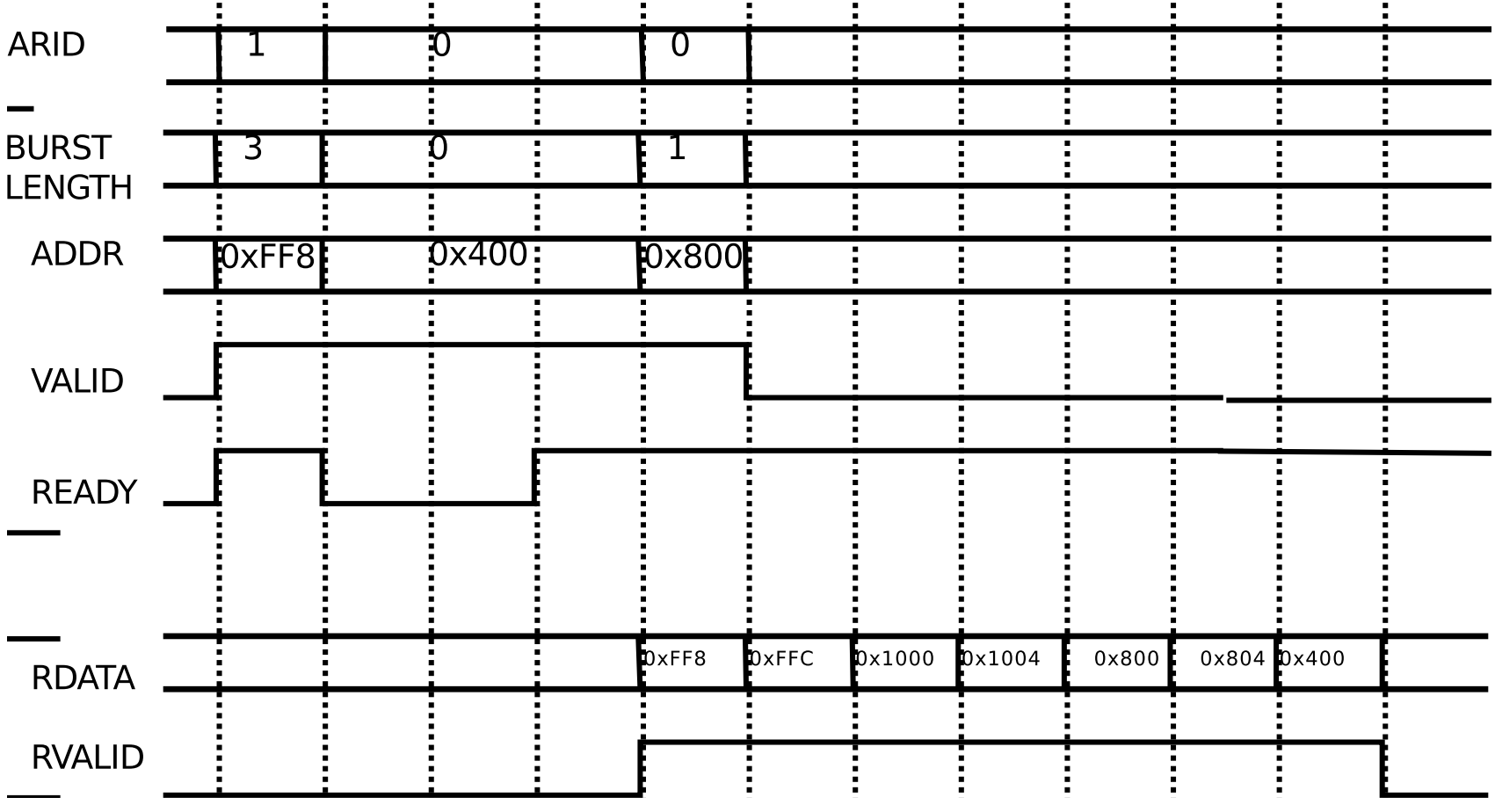
- Burstlength for incremental bursts can be 256 (16 for AXI3).
- Additional signal AxQOS. (x=RD/WR) 4 bit signal, higher value indicates higher priority
- Additional signal AxREGION. (x=RD/WR). Each memory mapped slave interface can be divided into regions (logical interfacs).
- Additional signal AxUSER. (x=RD/WR).

# AXI/OCP Differences

- No Separate WR/RD channel like AXI.
- A common command channel which issue both write/read commands.
- OCP can have several of the command channels in parallel. For multi-threading.
- Supports posted writes. (i.e no response required)

# Quiz

- Is there a Bug ?



# Plan

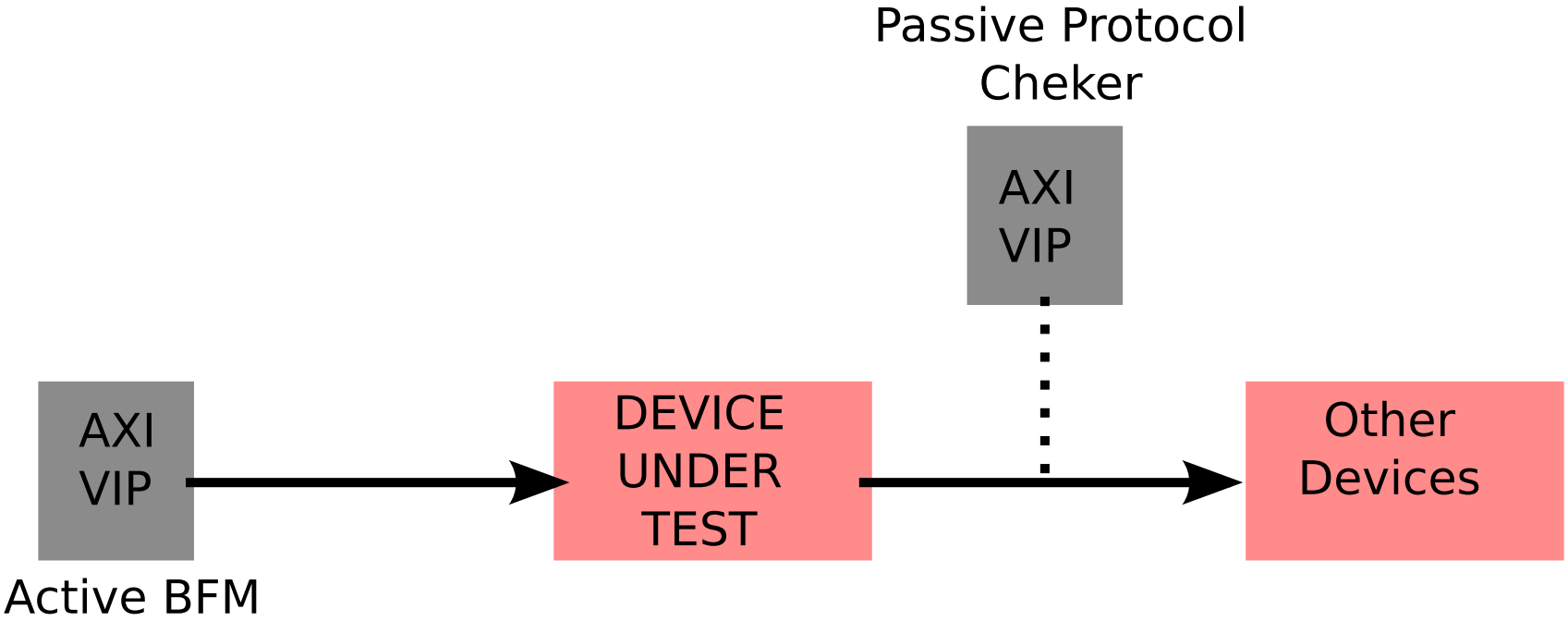
# Executable Specifications.

- AXI specifications are available as a set of SystemVerilog Assertions.
- Can be instantiated in the netlist for protocol checking.
- Can be synthesized into FPGA/Emulators.

# Constrained random verfication.

- Use VIPs(Verification IPs).
- Generate random AXI Traffic from a BFM (Bus Functional Master) towards IP interface.
- Constrain the traffic according to IP specs.
- Functional Coverage.
  - Need to check all possible combination of valid transactions.
  - e.g check burst length =(1,2,4,8) in each page of 4K in a 1M memory space. Need to hit $4 \times 256$ different cases.
  - Need to check that no rule is violated for all combinations.
- No Tape-out without  100% coverage.

# Constrained random verfication.



# Assertion based verfication.

- Use ABVIPs (Assertion Based Verification IPs).
- Can be used in Formal Verification Tools. (e.g Incisive Formal Verifier)
- In formal verification, functional coverage is 100% by definition.

# Plan

# References


- Amba specs.
  http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.set.amba/index.html.
- Cadence amba vips.
  http://www.cadence.com/downloads/rl/vip/AMBA.pdf.
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- Sudeep Pasricha and Nikil Dutt.
  *On-Chip Communication Architectures : System on Chip Interconnect*.
  Morgan Kaufmann Publishers Inc., San Francisco, CA, USA, 2008.