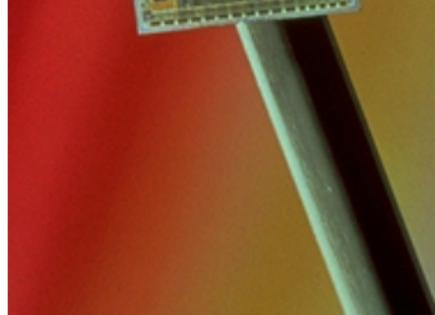




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# ICS904/EN2 : Design of Digital Integrated Circuits

L5 : Design automation : The "liberty" file  
format

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# Standard Cell characterization

## "Liberty" files

- Give all necessary informations to the synthesis and P&R tools
- A de-facto standard : "Liberty" files from "Synopsys" company.
- For each cell :
  - Logic behavior
  - Area
  - Power Consumption
  - Timing
- But also, for a whole library :
  - Characterization conditions (Process, Supply Voltage , Temperature)
  - Characterization conditions (Max rising time, Max capacitances,...)
  - Statistical capacitance model for wiring...

# An example library

## Nangate 45nm Open Cell Library

- Nangate is company creating characterization tools for standard cell libraries.
- Library distributed by Si2 (Silicon Integration Initiative) an association of electronic design automation companies.
- No way to process any true circuit, but usable for research and teaching purposes.
- Based on the NCSU (North Carolina State University) FreePDK45 process kit.
- FreePDK45 : An open source fictitious, non manufacturable process.



# Nangate 45nm Open Cell Library

## Units for measurements

```
/* Units Attributes */  
voltage_unit          : "1V";  
current_unit          : "1mA";  
pulling_resistance_unit : "1kohm";  
capacitive_load_unit    (1, ff);
```

- All measurements use defined units.

# Nangate 45nm Open Cell Library

## Characterization conditions

```
/* Operation Conditions */  
nom_process           : 1.00;  
nom_temperature       : 25.00;  
nom_voltage           : 1.10;  
  
voltage_map (VDD,1.10);  
voltage_map (VSS,0.00);
```

- Supply and ground nodes have a name...

# Nangate 45nm Open Cell Library

## "Corners" : Process, Voltage, Temperature

```
define(process_corner, operating_conditions, string);  
operating_conditions (typical) {  
    process_corner : "TypTyp";  
    process        : 1.00;  
    voltage        : 1.10;  
    temperature    : 25.00;  
    tree_type      : balanced_tree;  
}  
default_operating_conditions : typical;
```

- Several liberty files may be loaded at the same time by the tools (synthesis, P&R)
- For each kind of analysis, the appropriate "PVT" corner is chosen by the tool.
- For example a "worst case" corner is used for Tsetup analysis.
- For example a "best case" corner is used for Thold analysis.

# Nangate 45nm Open Cell Library

## Voltage thresholds for timing analysis

```
/* Threshold Definitions */  
slew_lower_threshold_pct_fall    : 30.00 ;  
slew_lower_threshold_pct_rise    : 30.00 ;  
slew_upper_threshold_pct_fall    : 70.00 ;  
slew_upper_threshold_pct_rise    : 70.00 ;  
input_threshold_pct_fall         : 50.00 ;  
input_threshold_pct_rise         : 50.00 ;  
output_threshold_pct_fall        : 50.00 ;  
output_threshold_pct_rise        : 50.00 ;
```

- Thresholds (fraction of the full range power supply) for logic level detection.
- Rising or Falling time of signal transition.
- Propagation time.

# Nangate 45nm Open Cell Library

## Default maximum values for capacitors and transition

```
default inout pin cap      : 1.000000;  
default input pin cap      : 1.000000;  
default output pin cap     : 0.000000;  
default fanout load        : 1.000000;  
default max transition      : 0.198535;
```

- Default input capacitor, load capacitor or fanout values of gates.
- Warning : The default maximum transition time is a constraint.
  - An arbitrary value chosen by the library designers.
  - Followed by the synthesis tool (or not ...)
  - Guarantees the validity domain of the timing characterization of library's gates.
  - **QUESTION** : what compromises are made when choosing this constraint ?

# Nangate 45nm Open Cell Library

## Wires model

```
wire_load("1K_hvratio_1_4") {  
    capacitance : 1.774000e-01;  
    resistance : 3.571429e-03;  
    slope : 5.000000;  
    fanout_length( 1, 1.3207 );  
    fanout_length( 2, 2.9813 );  
    fanout_length( 3, 5.1135 );  
    fanout_length( 4, 7.6639 );  
    fanout_length( 5, 10.0334 );  
    fanout_length( 6, 12.2296 );  
    fanout_length( 8, 19.3185 );  
}  
wire_load(....){...}  
...  
default_wire_load : "5K_hvratio_1_1" ;
```

- Allowing the synthesizer to estimate wire loads.
- A statistical model based on real circuits.
- $R = \text{resistance} * \text{fanout\_length}(\text{fanout})$
- $C = \text{capacitance} * \text{fanout\_length}(\text{fanout})$
- Several models based on circuit topology.
- Default model : 5K gates / form factor 1

# Nangate 45nm Open Cell Library

## Table templates for measurements

- Timings and power values are tabulated (no analytical model)
- Table interpolation for arbitrary input variables.

```
power_lut_template (Hidden_power_7) {  
    variable_1 : input_transition_time;  
    index_1 ("0.0010,0.0020,0.0030,0.0040,0.0050,0.0060,0.0070")  
}
```

- Example table template for power consumption measurement
- Named Hidden\_power\_7
- Input variable is a transition time
- 7 measurement points for 7 transition time values

# Nangate 45nm Open Cell Library

## A table template for propagation time

```
lu_table_template (Timing_7_7) {  
    variable_1 : input_net_transition;  
    variable_2 : total_output_net_capacitance;  
    index_1 ("0.0010,0.0020,0.0030,0.0040,0.0050,0.0060,0.0070");  
    index_2 ("0.0010,0.0020,0.0030,0.0040,0.0050,0.0060,0.0070");  
}
```

- Propagation time is a function of :

- The transition time of the input signal causing the output transition.
- The out load capacitance.
- $7 \times 7 = 49$  measurement points.

# Nangate 45nm Open Cell Library

## NAND2\_X4 : global data

```
cell (NAND2_X4) {  
    drive_strength : 4;  
    area          : 2.394000;  
    pg_pin(VDD) {  
        voltage_name : VDD;  
        pg_type     : primary_power;  
    }...  
}
```

- Global info on the cell
- General info on output buffers .(integer 1,2,4,8...)
- The synthesizer uses area info in order to optimize global synthesized area.
- All signals should be known, even supplies and grounds.

## NAND2\_X4 : Leakage power

```
cell_leakage_power : 69.573240;  
leakage_power () {  
    when           : "!A1 & !A2";  
    value          : 13.930180;  
}  
leakage_power () {  
    when           : "!A1 & A2";  
    value          : 99.197450;  
}  
leakage_power () {  
    when...
```

- The leakage power (Watts...) of the cell is a function of the internal state of the cell
- One mean value
- 4 values for the 4 entries in the truth table of the gate

# Nangate 45nm Open Cell Library

## NAND2\_X4 : An input signal : A1

```
pin (A1) {  
    direction      : input;  
    related_power_pin : "VDD";  
    related_ground_pin : "VSS";  
    capacitance    : 5.954965;  
    fall_capacitance : 5.698021;  
    rise_capacitance : 5.954965;  
}
```

- A1 is an input
- A1 has an input capacitance.
- A mean value of the input capacitance is given
- An input capacitance when A1 is falling.
- An different input capacitance when A1 is rising.

- **QUESTION** : Why two different input capacitances ?

# Nangate 45nm Open Cell Library

## NAND2\_X4 : An output signal : ZN

```
pin (ZN) {  
    direction : output;  
    related_power_pin : "VDD";  
    related_ground_pin : "VSS";  
    max_capacitance : 237.427000;  
    function : "!(A1 & A2)";
```

- ZN is an output
- The boolean equation is given (for synthesis...)
- Remember that the NAND2\_X4 gate has a max fanout of 4.
- The max capacitance for a X1 gate is  $59.3567fF$
- The max load capacitance a X4 gate is four times this value.

- **QUESTION** : Is it coherent with the max transition time ?

# Nangate 45nm Open Cell Library

## NAND2\_X4 : propagation time between A1 and ZN

```
timing () {
    related_pin    : "A1";
    timing_sense   : negative_unate;
    cell_fall(Timing_7_7) {
        index_1 ("0.00117378,0.00472397,0.0171859,0.0409838,0.0780596,0.130081,0.198535");
        index_2 ("0.365616,7.419590,14.839200,29.678400,59.356800,118.714000,237.427000");
        values ("0.00616709,0.00999692,0.0139268,0.0217239,0.0372647,0.0683098,0.130380", \
                 "0.00734947,0.0112111,0.0151774,0.0230153,0.0385880,0.0696532,0.131734", \
                 "0.00995234,0.0155306,0.0201539,0.0279856,0.0435159,0.0745711,0.136650", \
                 "0.0111666,0.0189948,0.0256394,0.0365212,0.0535191,0.0842981,0.146225", \
                 "0.0108485,0.0208434,0.0293531,0.0434564,0.0658692,0.100138,0.161536", \
                 "0.00880319,0.0209282,0.0312687,0.0484222,0.0759517,0.118635,0.183723", \
                 "0.00494015,0.0190727,0.0312259,0.0514041,0.0838078,0.134588,0.211792");
    }
    cell_rise(Timing_7_7) {
```

- related\_pin : which is the input pin causing the output transition ?
- timing\_sense : The output transition has not the same direction as the input transition.
- cell\_fall : Propagation time for a falling output.
- Reference to the Timing\_7\_7 (transition,load) template.
- First index related to line. Second Index related to column.

# Nangate 45nm Open Cell Library

## NAND2\_X4 : propagation time between A1 and ZN

```
timing () {
    related_pin      : "A1";
    timing_sense    : negative_unate;
    cell_fall(Timing_7_7) {
        index_1 ("0.00117378,0.00472397,0.0171859,0.0409838,0.0780596,0.130081,0.198535");
        index_2 ("0.365616,7.419590,14.839200,29.678400,59.356800,118.714000,237.427000");
        values ("0.00616709,0.00999692,0.0139268,0.0217239,0.0372647,0.0683098,0.130380", \
                 "0.00734947,0.0112111,0.0151774,0.0230153,0.0385880,0.0696532,0.131734", \
                 "0.00995234,0.0155306,0.0201539,0.0279856,0.0435159,0.0745711,0.136650", \
                 "0.0111666,0.0189948,0.0256394,0.0365212,0.0535191,0.0842981,0.146225", \
                 "0.0108485,0.0208434,0.0293531,0.0434564,0.0658692,0.100138,0.161536", \
                 "0.00880319,0.0209282,0.0312687,0.0484222,0.0759517,0.118635,0.183723", \
                 "0.00494015,0.0190727,0.0312259,0.0514041,0.0838078,0.134588,0.211792");
    }
    cell_rise(Timing_7_7) {
```

- Index values are redefined.
- Note : max transition < default\_max\_transition.
- Note : max capa < max\_capacitance.
- Same kind of table for a rising transition of the output.
- Same kind of table for each path from any input to any output.

# Nangate 45nm Open Cell Library

## NAND2\_X4 : Falling Transition time of ZN signal

```
fall_transition(Timing_7_7) {
    index_1 ("0.00117378,0.00472397,0.0171859,0.0409838,0.0780596,0.130081,0.198535");
    index_2 ("0.365616,7.419590,14.839200,29.678400,59.356800,118.714000,237.427000");
    values ("0.00313418,0.00633765,0.00970606,0.0164353,0.0298921,0.0567985,0.110610", \
            "0.00315002,0.00633771,0.00970602,0.0164361,0.0298928,0.0567975,0.110614", \
            "0.00594783,0.00855601,0.0108711,0.0165314,0.0298930,0.0567989,0.110613", \
            "0.0100557,0.0135596,0.0166079,0.0217381,0.0314545,0.0568000,0.110613", \
            "0.0155905,0.0199433,0.0237401,0.0301861,0.0406656,0.0599695,0.110612", \
            "0.0227162,0.0279150,0.0324341,0.0400918,0.0526945,0.0727865,0.113484", \
            "0.0316036,0.0376134,0.0428795,0.0517033,0.0662647,0.0896769,0.127281");
}
```

- Reference to the Timing\_7\_7 (transition,load) template
- Same kind of table for a rising transition of the output.
- Coherency : The maximum transition time (0.127281) is less than the default\_max\_transition

# Nangate 45nm Open Cell Library

## NAND2\_X4 : Internal Dynamic power consumption of the gate

```
internal_power () {
    related_pin      : "A1";
    fall_power(Power_7_7) {
        index_1 ("0.00117378,0.00472397,0.0171859,0.0409838,0.0780596,0.130081,0.198535");
        index_2 ("0.365616,7.419590,14.839200,29.678400,59.356800,118.714000,237.427000");
        values ("0.795787,0.940878,0.980508,1.014321,1.042872,1.047780,1.052940", \
                 "0.527188,0.716998,0.831193,0.921873,0.985745,1.018615,1.041402", \
                 "0.838523,0.654409,0.697793,0.801639,0.888976,0.958862,1.007789", \
                 "2.454897,1.823314,1.436914,1.141771,1.072669,1.059437,1.049585", \
                 "5.068604,4.189000,3.531058,2.676582,1.933285,1.575694,1.350992", \
                 "8.605884,7.786085,6.914839,5.578610,4.057340,2.851663,2.142791", \
                 "13.235730,12.471150,11.622380,9.965538,7.625804,5.289704,3.673908");
    }
}
```

- Internal energy consumption (Joules...) used for a fall transition of Z1 caused by a A1 transition .
- Correlated with the input transition time and the capacitive load.
- All cases should be tabulated...
- **Warning** : This doesn't take into account the energy stored in the load capacitor itself.
- **Question** : How to explain this kind of measurements ?.



# Nangate 45nm Open Cell Library

## DFF\_X2 : Global data

```
cell (DFF_X2) {  
    drive_strength      : 2;  
    ff ("IQ" , "IQN") {  
        next_state       : "D";  
        clocked_on       : "CK";  
    }  
}
```

- Global information on the cell
- Buffer size X2
- The gate is a D flip-flop working on the rising edge of CK
- The gate has two outputs Q and QN

# Nangate 45nm Open Cell Library

## DFF\_X2 : Leakage Power

```
cell_leakage_power : 115.103670;  
  
leakage_power () {  
    when : "!CK & !D & !Q & QN";  
    value : 107.651390;  
}  
leakage_power () {  
    when : "!CK & !D & Q & !QN";  
    value : 115.805800;  
}  
...  
...
```

- The leakage power is a function of the state of the cell.
- A mean value.
- As the cell is sequential the leakage power is also a function of the outputs !!.
- Here 8 cases have to be measured.

# Nangate 45nm Open Cell Library

## DFF\_X2 : Hold constraint on the D input

```
timing () {  
    related_pin      : "CK";  
    timing_type      : hold_rising;  
    fall_constraint(Hold_3_3) {  
        index_1 ("0.00117378,0.0449324,0.198535");  
        index_2 ("0.00117378,0.0449324,0.198535");  
        values ("0.000950,0.009897,0.009901", \  
                "0.004801,0.011035,0.005683", \  
                "0.144217,0.153663,0.144977");  
    }  
}
```

- "Hold time" from rising of clk for a rising transition of D.
- Tabulated (Hold\_3\_3)
- Index 1 : Transition time of D
- Index 2 : Transition time of CK
- Same kind of table for the "Setup Time".

- **QUESTION** : What about the output load capacitance ?

# Nangate 45nm Open Cell Library

## DFF\_X2 : Hidden power for a transition of D

```
internal_power () {  
    when           : "!CK & !Q & QN";  
  
    fall_power(Hidden_power_7) {  
        index_1 ("0.00117378,0.00472397,0.0171859,0.0409838,0.0780596,0.130081,0.198535");  
        values ("4.354644,4.333607,4.304507,4.328622,4.507989,4.894921,5.519367");  
    }  
    rise_power(Hidden_power_7) {  
        index_1 ("0.00117378,0.00472397,0.0171859,0.0409838,0.0780596,0.130081,0.198535");  
        values ("3.211098,3.175770,3.145376,3.177001,3.349767,3.724420,4.327453");  
    }  
}  
}  
...
```

- Energy used for a transition of D (no transition on CLK or the outputs)
- Depends only on then transition time of D.
- **Warning** : Doesn't take into account energy stored in the input capacitance itself.
- 4x2 cases linked to the state of the flip-flop and the value of CK.

# Nangate 45nm Open Cell Library

## DFF\_X2 : CK clock constraints

```
...
clock      : true;
...
timing () {
    related_pin      : "CK";
    timing_type      : min_pulse_width;
    fall_constraint(Pulse_width_3) {
        index_1 ("0.00117378,0.0449324,0.198535");
        values ("0.054590,0.069863,0.198733");
    }
    rise_constraint(Pulse_width_3) {
        index_1 ("0.00117378,0.0449324,0.198535");
        values ("0.080840,0.080924,0.198733");
    }
}
...
internal_power() {...}
...
```

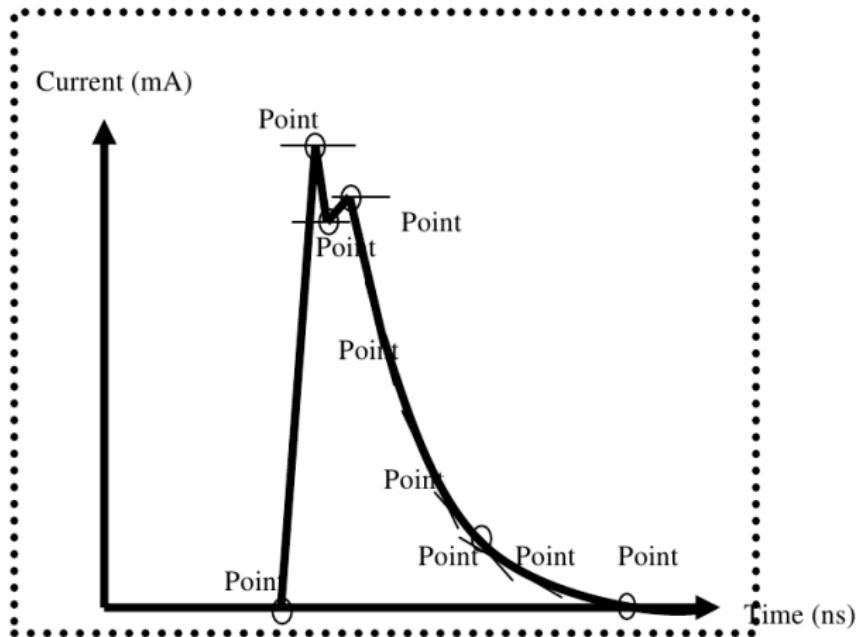
- CK is clock...
- The minimum duration of the "1" state is tabulated.
- This duration is a function of the transition time of the clock.
- With hidden power consumption when D and Q are identical...

- **Warning :** All events on outputs are related to the CK transition
- Transition times are functions of the CK transition time and of the output load capacitance.
- Propagation times are functions of the CK transition time and of the output load capacitance.
- Power consumption tabulated for transition of Q due to a transition of CK.

- The examined NLDM model (Non Linear Delay Model) is not enough accurate for recent technologies.
- "IR drop" simulation needs a more sophisticated model.
- Evolution proposed par Synopsys (CCS pour Composite Current Source).
- Evolution proposed par Cadence (ECSM pour Effective Current Source Model).

# Liberty files

## Cadence ECSM : the model

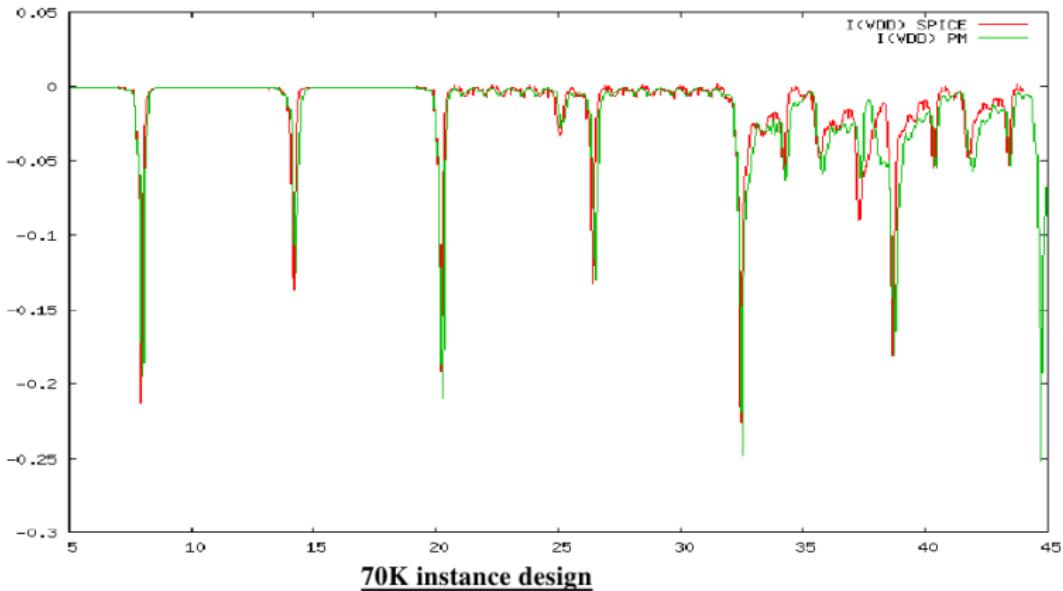


Src. Cadence Design Systems.



# Liberty files

## Cadence ECSM : IRDROP simulation



Src. Cadence Design Systems.

- The input capacitance is tabulated.
- The output model is a non linear current or voltage source
- Current/Voltages are tabulated as functions of time.
- Complex models but results near electrical simulation results...
- The 3 kind of models are distributed for the foundries clients (NLDM :51Mo, ECSM :291Mo, CCS :781Mo)



# Liberty files

## Why a lecture on this syntax ?

- The designer may add it's own macro-cells to existing libraries.
- From time to time, the designer have to tweak the liberty file in order to have correct behavior.
- In hierarchical designs, tools may generate black-box Liberty files at the block level.
- In order write efficients synthesis scripts:.